MAR ATHANASIUS COLLEGE OF ENGINEERING

(Government Aided & Autonomous)

Kothamangalam 686 666

Affiliated to APJ Abdul Kalam Technological University

Thiruvananthapuram

Master of Technology (M. Tech)

Curriculum - 2024

COLLEGE VISION AND MISSION

VISION

Excellence in education through resource integration.

MISSION

The institution is committed to transform itself into a centre of excellence in Technical Education upholding the motto "Knowledge is Power."

This is to be achieved by imparting quality education to mould technically competent professionals with moral integrity, ethical values and social commitment, and by promoting innovative activities in the thrust areas emerging from time to time

MAR ATHANASIUS COLLEGE OF ENGINEERING

(GOVT. AIDED & AUTONOMOUS)

M.TECH CURRICULUM AND SCHEME-2024

Department of Electronics and Communication Engineering

(VLSI and Embedded Systems)

PROGRAM OUTCOMES – PO

Outcomes are the attributes that are to be demonstrated by a graduate after completing the programme

PO1: An ability to independently carry out research/investigation anddevelopment work in engineering and allied streams

PO2: An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.

PO3: An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PO4: An ability to apply stream knowledge to design or develop solutions for realworld problems by following the standards

PO5: An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tool to model, analyse and solve practical engineeringproblems.

PO6: An ability to engage in life-long learning for the design and development of the stream related problems taking into consideration sustainability, societal, ethical and environmental aspects. Also to develop cognitive skills for project management and finance which focus on Industry and Entrepreneurship.

The departments conducting the M.Tech programme shall define their own PSOs, if required, and evaluation shall also be done for the same.

SEMESTER I

Slot	Course Code	Course	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
A	M24EC1T101	Digital CMOS VLSI Design	40	60	4-0-0-4	4	4
B	M24EC1T102	FPGA-Based System Design	40	60	4-0-0-4	4	4
C	M24EC1T103	Design with Advanced Microcontroller	40	60	4-0-0-4	4	4
D	M24EC1E104A	Programme Elective1	40	60	3-0-0-3	3	3
E	M24EC1E105A	Programme Elective2	40	60	3-0-0-3	3	3
J	M24EC1R106	Research Methodology & IPR	40	60	2-0-0-2	2	2
G	M24EC1L107	HDL Lab	60	40	0-0-3-3	3	2
	Total		300	400		23	22

Teaching Assistance: 7 hours

Self-study- 23 Hrs

Programme Elective 1

Slot	Course Code	Course	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
D	M24EC1E104A	Physical Design Automation	40	60	3-0-0-3	3	3
D	M24EC1E104B	EDA tools	40	60	3-0-0-3	3	3
D	M24EC1E104C	DSP Algorithms and Architecture	40	60	3-0-0-3	3	3
D	M24EC1E104D	Advanced Digital Signal Processing	40	60	3-0-0-3	3	3
D	M24EC1E104E	Electronic Packaging	40	60	3-0-0-3	3	3

Programme Elective 2

Slot	Course Code	Course	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
E	M24EC1E105A	Advanced Digital System Design	40	60	3-0-0-3	3	3
E	M24EC1E105B	Digital Design Principles and Applications	40	60	3-0-0-3	3	3
E	M24EC1E105C	Functional verification with system Verilog	40	60	3-0-0-3	3	3
E	M24EC1E105D	ASIC design	40	60	3-0-0-3	3	3
E	M24EC1E105E	Embedded Operating system	40	60	3-0-0-3	3	3

SEMESTER – II

Slot	Course Code	Course	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
A	M24EC1T201	Analog VLSI Design	40	60	4-0-0-4	4	4
B	M24EC1T202	Sensor Technologies and MEMS	40	60	4-0-0-4	4	4
C	M24EC1E203A	Programme Elective 3	40	60	3-0-0-3	3	3
D	M24EC1E204A	Programme Elective 4	40	60	3-0-0-3	3	3
E	M24EC1S205	Industry Integrated Course	40	60	3-0-0-3	3	3
G	M24EC1P206	Mini Project	60	40	0-0-3-3	3	2

Teaching Assistance: 7 hours

H	M24EC1L207	Advanced Microcontroller Lab	60	40	0-0-3-3	3	2
	Total		320	380		23	21

Self-study- 23 Hrs

Programme Elective 3

Slot	Course Code	Course	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
C	M24EC1E203A	Embedded Networking	40	60	3-0-0-3	3	3
C	M24EC1E203B	SOC Design	40	60	3-0-0-3	3	3
C	M24EC1E203C	VLSI structure for DSP	40	60	3-0-0-3	3	3
C	M24EC1E203D	Semiconductor Memories	40	60	3-0-0-3	3	3
C	M24EC1E203E	Embedded System Design	40	60	3-0-0-3	3	3

Programme Elective 4

Slot	Course Code	Course	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
D	M24EC1E204A	Low Power VLSI	40	60	3-0-0-3	3	3
D	M24EC1E204B	VLSI System Testing	40	60	3-0-0-3	3	3
D	M24EC1E204C	High Speed Digital Design	40	60	3-0-0-3	3	3
D	M24EC1E204D	Deep Learning	40	60	3-0-0-3	3	3
D	M24EC1E204E	Static Timing Analysis	40	60	3-0-0-3	3	3

SEMESTER - III

TRACK 1							
Slot	Course Code	Course	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
A	M24EC1M301	*MOOC	To be completed successfully		--		2
B	M24EC1E302A	Programme Elective5	40	60	3-0-0-3	3	3
K	M24EC1I303	**Internship	50	50	--	-	3
P	M24EC1P304	Dissertation Phase 1	100	--	0-0-16-16	16	11
	Total		190	110		19	19

TRACK 1I							
A	M24EC1M305	* MOOC 1	To be completed successfully		--	--	2
B	M24EC1M306	* MOOC 2	To be completed successfully		--	--	2
K	M24EC1I307	## Internship	50	50	--	--	4
P	M24EC1P308	###Dissertation Phase 1	100	--	--	--	11
	Total		150	50			19

Programme Elective 5

Slot	Course Code	Course	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
B	M24EC1E302A	Embedded Systems for Automotive Application	40	60	3-0-0-3	3	3
B	M24EC1E302B	Embedded Systems for Robotics	40	60	3-0-0-3	3	3
B	M24EC1E302C	Machine Learning for Embedded Applications	40	60	3-0-0-3	3	3
B	M24EC1E302D	IoT Based Embedded Systems	40	60	3-0-0-3	3	3
B	M24EC1E302E	Embedded Systems in Smart Grid	40	60	3-0-0-3	3	3

Teaching Assistance: 7 hours

*MOOC Course of minimum 8 weeks duration to be successfully completedbefore the end of fourth semester (starting from semester 1).

**Internship- mandatory internship of 6 to 8 weeks

Internship - mandatory internship of more than 16 weeks

###Dissertation Phase 1 – Should be done in Industry

TRACK 1 / TRACK 2

In second year, the students can choose either of the two tracks: TRACK 1 or TRACK 2. Track 1 is conventional M.Tech programme in which the dissertation Phase 1 is conducted in college. Track 2 is M.Tech programme designed for students who undergone long term internship (not less than 16 weeks) in industry. An aspirant in track 2 needs to do the dissertation in the industry. The candidates should also be good with performing in-depth research and colluding the conclusions of research led by them. Such students are expected to have the following skills: Technical Skills, Research Skills, Communication Skills, Critical Thinking Skills, and Problem-Solving Skills.

The eligibility for Track 2:

- Shall have qualified in the GATE or have a SGPA above 8.0 during thefirst semester, and
- Qualify an interview during the end of second semester by anexpert committee constituted by the College.

SEMESTER – IV

TRACK 1							
Slot	**Course Code**	**Course**	**Marks**		**L-T-P-S**	**Hours**	**Credit**
			CIE	**ESE**			
P	**M24EC1P401**	**Dissertation Phase II**	**100**	**100**	**0-0-27-24**	**27**	**18**
	Total		**100**	**100**		**27**	**18**
TRACK 1I							
P	**M24EC1P402**	**##Dissertation Phase II**	**100**	**100**			**18**
	Total		**100**	**100**			**18**
	Total credits in all four semesters						**80**

##Dissertation Phase II- Should be done in Industry

COURSE NUMBERING SCHEME

The course number consists of digits/alphabets. The pattern to be followed is

The course number consists of digits/alphabets. The pattern to be followed is

For General Courses- MYYBBXCSNNFor Elective Courses - MYYBBXCSNNA

- M: MASTERS
- YY: Last two digits of year of regulation
- BB: DEPARTMENT

Sl. No	Department	CoursePrefix
01	Civil Engg	CE
02	Computer Science	CS
03	Electrical& Electronics	EE
04	Electronics & Communication	EC
05	Mechanical Engg	ME
06	Any	GE
07	External (Industry/N PTEL etc)	EX

- X :Specialization number
- S : Semester of Study

2- Semesters 1

3- Semester 2

4- Semester 3

5- Semester 4

- C: Course Type

T- Core Course

E- Elective Course

R- Research Methodology & IPRL- Laboratory Course

S- Industry Integrated CourseI- Internship

M- MOOC

P- Project/Dissertation

- NN: Course sequence number
- A: Elective sequence number - A/B/C/D/E It is illustrated below: Examples:

M24CE1T202 is a second core course of first specialization offered by the CivilDepartment

in semester 2

M24EC1R106 is Research Methodology & IPR offered in semester 1

M24EC1E104A is the first subject of Elective 1 of first specialization offered by the EC Department in semester 1

EVALUATION PATTERN

(i) CORE COURSES

Evaluation shall only be based on application, analysis or design based questions (for both internal and end semester examinations).

Continuous Internal Evaluation: 40 marks

Micro project/Course based project	:	10 marks
Course based task/Seminar/Quiz	:	10 marks
Test paper 1 (Module 1 and Module 2)	:	10 marks
Test paper 2 (Module 3 and Module 4)	:	10 marks

The project shall be done individually (Preferable).

End Semester Examination : 60marks

The end semester the college will conduct examination. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total durationof the examination will be 3 Hrs.

(ii) ELECTIVE COURSES

Evaluation shall only be based on application, analysis or design based questions (for both internal and end semester examinations).

Continuous Internal Evaluation: 40 marks

Seminar* : 10 marks

Course based task/Micro Project//Data

Collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination: 60 marks

The end semester the College will conduct examination. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 4 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

(iii) RESEARCH METHODOLOGY & IPR

Continuous Internal Evaluation: 40 marks

Preparing a review article based on peer reviewed Original publications in the relevant discipline (minimum 10 Publications shall be referred) : 10 marks

Course based task/Seminar/Quiz : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

End Semester Examination : 60 marks

The end semester examination should be conducted by the college. The time duration will be for 3 Hrs and will contain 7 questions, with minimum one question from each module of which student should answer any five. Each question can carry 12 marks.

(iv) INTERNSHIP

Internships are educational and career development opportunities, providing practical experience in a field or discipline. They are structured, short-term, supervised placements often focused around particular tasks or projects with defined timescales. An internship may be compensated or non-compensated by the organization providing the internship. The internship has to be meaningful and mutually beneficial to the intern and the organization. It is important that the objectives and the activities of the internship program are clearly defined and understood. The internship offers the students an opportunity to gain hands-on industrial or organizational exposure; to integrate the knowledge and skills acquired through the coursework; interact with professionals and other interns; and to improve their presentation, writing, and communication skills. Internship often acts as a gateway for final placement for many students.

A student shall opt for carrying out the Internship at an Industry/Research Organization or at another institute of higher learning and repute (Academia). The organization for Internship shall be selected/decided by the students on their own with prior approval from the faculty advisor/respective PG Programme Coordinator/Guide/Supervisor. Every student shall be assigned an internship Supervisor/Guide at the beginning of the Internship. The training shall be related to their specialization after the second semester for a minimum duration of six to eight weeks. On completion of the course, the student is expected to be able to develop skills in facing and solving the problems experiencing in the related field.

Objectives

- Exposure to the industrial environment, which cannot be simulated in the classroom and hence creating competent professionals for the industry.
- Provide possible opportunities to learn understand and sharpen the real time technical / managerial skills required at the job.
- Exposure to the current technological developments relevant to the subject area of training.
- Create conducive conditions with quest for knowledge and its applicability on the job.
- Understand the social, environmental, economic and administrative considerations that influence the working environment.

- Expose students to the engineer's responsibilities and ethics.

Benefits of Internship

Benefits to Students

- An opportunity to get hired by the Industry/ organization.
- Practical experience in an organizational setting & Industry environment.
- Excellent opportunity to see how the theoretical aspects learned in classes are integrated into the practical world. On-floor experience provides much more professional experience which is often worth more than classroom teaching.
- Helps them decide if the industry and the profession is the best career optionto pursue.
- Opportunity to learn new skills and supplement knowledge.
- Opportunity to practice communication and teamwork skills.
- Opportunity to learn strategies like time management, multi-tasking etc in an industrial setup.
- Makes a valuable addition to their resume.
- Enhances their candidacy for higher education/placement.
- Creating network and social circle and developing relationships with industry people.
- Provides opportunity to evaluate the organization before committing to afull time position.

Benefits to the Institute

- Build industry academia relations.
- Makes the placement process easier.
- Improve institutional credibility & branding.
- Helps in retention of the students.
- Curriculum revision can be made based on feedback from Industry/students.
- Improvement in teaching learning process.

Benefits to the Industry

- Availability of ready to contribute candidates for employment.
- Year round source of highly motivated pre-professionals.
- Students bring new perspectives to problem solving.
- Visibility of the organization is increased on campus.
- Quality candidate's availability for temporary or seasonal positions andprojects.
- Freedom for industrial staff to pursue more creative projects.
- Availability of flexible, cost-effective workforce not requiring a longtermemployer commitment.
- Proven, cost-effective way to recruit and evaluate potential employees.
- Enhancement of employer's image in the community by contributing to theeducational enterprise.

Types of Internships

- Industry Internship with/without Stipend
- Govt / PSU Internship (BARC/Railway/ISRO etc)
- Internship with prominent education/research Institutes
- Internship with Incubation centres /Start-ups

Guidelines

- All the students need to go for internship for minimum duration of 6 to 8 weeks.
- Students can take mini projects, assignments, case studies by discussing it with concerned authority from industry and can work on it during internship.
- All students should compulsorily follow the rules and regulations as laid byindustry.
- Every student should take prior permissions from concerned industrial authority if they want to use any drawings, photographs or any other document from industry.
- Student should follow all ethical practices and SOP of industry.

- Students have to take necessary health and safety precautions as laid by theindustry.
- Student should contact his /her Guide/Supervisor from college on weeklybasis to communicate the progress.
- Each student has to maintain a diary/log book
- After completion of internship, students are required to submit
- Report of work done
- Internship certificate copy
- Feedback from employer / internship mentor
- Stipend proof (in case of paid internship).

Total Marks 100: The marks awarded for the Internship will be on the basis of (i)Evaluation done by the Industry (ii) Students diary (iii) Internship Report and (iv) Comprehensive Viva Voce.

Continuous Internal Evaluation: 50 marks

Student's diary - 25 Marks

Evaluation done by the Industry - 25 Marks

Student's Diary/ Daily Log: The main purpose of writing daily diary is to cultivate the habit of documenting and to encourage the students to search for details. It develops the students' thought process and reasoning abilities. The students shouldrecord in the daily training diary the day to day account of the observations, impressions, information gathered and suggestions given, if any. It should contain the sketches & drawings related to the observations made by the students. The dailytraining diary should be signed after every day by the supervisor/ in charge of the section where the student has been working. The diary should also be shown to the Faculty Mentor visiting the industry from time to time and got ratified on the day ofhis visit. Student's diary will be evaluated on the basis of the following criteria:

- Regularity in maintenance of the diary
- Adequacy & quality of information recorded
- Drawings, design, sketches and data recorded

- Thought processand recording techniques used
- Organization of the information.

The format of student's diary

Name of the Organization/Section:

Name and Address of the Section Head:

Name and Address of the Supervisor:

Name and address of the student:

Internship Duration: From ..... To .....

Brief description about the nature of internship:

Day	Brief write up about the Activities carried out: Such as design, sketches, result observed, issues identified, data recorded, etc.
1	
2	
3	

Signature of Industry Supervisor *Signature of Section Head/HR Manager*

Office Seal

Attendance Sheet

Name of the Organization/Section:

Name and Address of the Section Head:

Name and Address of the Supervisor:

Name and address of the student:

Internship Duration: From ..... To .....

Month & Year	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	...
Month & Year																					
Month & Year																					

Signature of Industry Supervisor *Signature of Section Head/HR Manager*

Office Seal

Note:

- Student's Diary shall be submitted by the students along with attendance record and an evaluation sheet duly signed and stamped by the industry to the Institute immediately after the completion of the training.

- Attendance Sheet should remain affixed in daily training diary. Do notremove or tear it off.
- Student shall sign in the attendance column. Do not mark 'P'.
- Holidays should be marked in red ink in the attendance column. Absentshould be marked as 'A' in red ink.

Evaluation done by the Industry (Marks 25)

Format for Supervisor Evaluation of Intern

Student Name :_____Date:__ Supervisor Name :_____Designation:__

Company/Organization :_____

Internship Address: _____ Dates of Internship: From___To

Please evaluate intern by indicating the frequency with which you observed following parameters:

Parameters Marks	Needs improvement (0 – 0.25 mark)	Satisfactory (0.25 –0.50 mark)	Good (0.75 mark)	Excellent (1 mark)
Behavior				
Performs in a dependable Manner				
Cooperates with coworkers and supervisor				
Shows interest in work				
Learns quickly				
Shows initiative				
Produces high quality work				
Accepts responsibility				
Accepts criticism				
Demonstrates organizational skills				
Uses technical knowledge and expertise				
Shows good judgment				
Demonstrates creativity/originality				
Analyzes problems effectively				
Is self-reliant				
Communicates well				
Writes effectively				

Has a professional attitude				
Gives a professional appearance				
Is punctual				
Uses time effectively				

Overall performance of student

Intern (Tick one) : Needs improvement (0 - 0.50 mark) / Satisfactory (0.50 – 1.0 mark) / Good (1.5 mark) / Excellent (2.0 mark)Additional comments, if any (2 marks) :

Signature of Industry Supervisor *Signature of Section Head/HRManager*

Office Seal

End Semester Evaluation (External Evaluation): 50 Marks

Internship Report - 25 Marks

Viva Voce - 25 Marks

Internship Report: After completion of the internship, the student should prepare a comprehensive report to indicate what he has observed and learnt in the training period and should be submitted to the faculty Supervisor. The student may contact Industrial Supervisor/ Faculty Mentor for assigning special topics andproblems and should prepare the final report on the assigned topics. Daily diary willalso help to a great extent in writing the industrial report since much of theinformation has already been incorporated by the student into the daily diary. The training report should be signed by the Internship Supervisor, Programme Coordinator and Faculty Mentor.

The Internship report (25 Marks) will be evaluated on the basis of following criteria:

- Originality
- Adequacy and purposeful write-up
- Organization, format, drawings, sketches, style, language etc.
- Variety and relevance of learning experience
- Practical applications, relationships with basic theory and concepts taughtin the

course

Viva Voce (25 Marks) will be done by a committee comprising Faculty Supervisor, PG Programme Coordinator and an external expert (from Industry or research/academic Institute). This committee will be evaluating the internship reportalso.

(v) LABORATORY COURSES

Lab work and Viva-voce : 60 marks

Final evaluation Test and Viva voce : 40 marks

The laboratory courses will be having only Continuous Internal Evaluation and carries 100 marks. Final evaluation shall be done by two examiners; one examiner willbe a senior faculty from the same department.

(vi) INDUSTRY INTEGRATED COURSE

Engineering students frequently aspire to work in areas and domains that are key topics in the industry. There are concerns by recruiters that skill sets of engineering students did not match with the Industry requirements, especially in the field of latesttopics. In response to their desires, the College has incorporated Industry integratedcourse in the curriculum.

The evaluation pattern for Industry based electives is as follows:

Continuous Internal Evaluation: 40 marks

Seminar : 10 marks

Course based task/Seminar/Data collection and interpretation/Case study : 10marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

End Semester Examination : 60 marks

The examination will be conducted by the College with the question paper provided by the Industry. The examination will be for 3 Hrs and will contain 7 questions, with minimum one question from each module of which student should answer any five. Each question can carry 12 marks. The valuation of the answer scripts shall be done by the expert in the Industry handling the course.

(vii) MOOC COURSES

The MOOC course shall be considered only if it is conducted by the agencies namely AICTE/NPTEL/SWAYAM or NITTTR. The MOOC course should have a minimum duration of 8 weeks and the content of the syllabus shall be enough for at least 40 hours of teaching. The course should have a proctored/offline end semester examination. The students can do the MOOC according to their convenience, but shall complete it before the end of fourth semester. The list of MOOC courses will be provided by the concerned BoS if at least 70% of the course content match with the area/stream of study. The course shall not be considered if its content has more than 50% of overlap with a core/elective course in the concerned discipline or with an open elective.

MOOC Course to be successfully completed before the end of fourth semester (starting from semester 1). A credit of 2 will be awarded to all students whoever successfully completes the MOOC course as per the evaluation pattern of the respective agency conducting the MOOC.

(viii) MINIPROJECT

Total marks: 100, only CIE

Mini project can help to strengthen the understanding of student's fundamentals through application of theoretical concepts and to boost their skills and widen the horizon of their thinking. The ultimate aim of an engineering student is to resolve a problem by applying theoretical knowledge. Doing more projects increases problem-solving skills. The introduction of mini projects ensures preparedness of students toundertake dissertation. Students should identify a topic of interest in consultation with PG Programme Coordinator. Demonstrate the novelty of the project through the results and outputs. The progress of the mini project is evaluated based on threereviews, two interim reviews and a final review.

A report is required at the end of the semester.

Interim evaluation: 40 (20 marks for each review), final evaluation by a Committee (will be evaluating the level of completion and demonstration of functionality/specifications, clarity of presentation, oral examination, work knowledge and involvement): 35, Report (the committee will be evaluating for the technical content, adequacy of references, templates followed and permitted plagiarism level is not more than 25%): 15, Supervisor/Guide: 10

(ix) DISSERTATION

Dissertation: All Students should carry out the dissertation in the college or can work either in any CSIR/Industrial R&D organization/any other reputed Institute which have facilities for dissertation work in the area proposed.

Dissertation outside the Institute: For doing dissertation outside the Institution, the following conditions are to be met:

- They have completed successfully the course work prescribed in the approved curriculum up to the second semester.
- They should choose Track 2 in semester 3 and 4
- The student has to get prior approval from the DLAC and CLAC.
- Facilities required for doing the dissertation shall be available in the Organization/Industry (A certificate stating the facilities available in the proposed organization and the time period for which the facilities shall be made available to the student, issued by a competent authority from the Organization/Industry shall be submitted by the student along with the application).
- They should have an external as well as an internal supervisor. The internal supervisor should belong to the parent institution and the external supervisor should be Scientists or Engineers from the Institution/Industry/ R&D organization with which the student is associated for doing thedissertation work. The external supervisor shall be with a minimum post graduate degree in the related area.
- The student has to furnish his /her monthly progress as well as attendance report

signed by the external guide and submit the same to the concerned Internal guide.

- The external guide is to be preferably present during all the stages of evaluation of the dissertation.

Note1- Students availing this facility should continue as regular students ofthe College itself.

Note 2-The course work in the 3rd semester is to be completed as per the curriculum requirements (i) MOOC can be completed as per the norms mentioned earlier

Internship leading to Dissertation: The M. Tech students who after completionof 6 to 8 weeks internship at some reputed organization are allowed to continue their work as dissertation for the third and fourth semester after getting approval from theDLAC. Such students shall make a brief presentation regarding the work they propose to carry out before the DLAC for a detailed scrutiny and to resolve its suitability for accepting it as an M.Tech dissertation. These students will be continuing as regular students of the Institute in third semester for carrying out all academic requirements as per the curriculum/regulation. However, they will be permitted to complete their dissertation in the Industry/Organization (where they have successfully completed their internship) during fourth semester.

Dissertation as part of Employment: Students may be permitted to discontinue the programme and take up a job provided they have completed all the courses till second semester (FE status students are not permitted) prescribed in the approved curriculum. The dissertation work can be done during a later period either in the organization where they work if it has R & D facility, or in the Institute. Such students should submit application with details (copy of employment offer, plan of completion of their project etc.) to the Dean (PG) through HoD. The application shallbe vetted by CLAC before granting the approval. When the students are planning todo the dissertation work in the organization with R & D facility where they are employed, they shall submit a separate application having following details:

- Name of R&D Organization/Industry
- Name and designation of an external supervisor from the proposed Organization/Industry (Scientists or Engineers with a minimum post graduate degree in the related area) and his/her profile with consent

- Name and designation of a faculty member of the Institute as internal supervisor with his/her consent
- Letter from the competent authority from the Organization/Industry granting permission to do the dissertation
- Details of the proposed work
- Work plan of completion of project

DLAC will scrutinize the proposal and forward to CLAC for approval.

When students are doing dissertation work along with the job in the organization(with R & D facility) where they are employed, the dissertation work shall be completed in four semesters normally (two semesters of dissertation work along with the job may be considered as equivalent to one semester of dissertation work at the Institute). Extensions may be granted based on requests from the student and recommendation of the supervisors such that he/she will complete the M. Tech programme within four years from the date of admission as per the regulation. Method of evaluation and grading of the dissertation will be the same as in the caseof regular students. The course work in the 3rd semester for such students are to be completed as per the curriculum requirements (i) MOOC can be completed as per the norms mentioned earlier. However, for self learning students, all evaluations shall be carried out in their parent Institution as in the case of regular students.

Mark Distribution:

Phase 1: Total marks: 100, only CIE

Phase 2: Total marks: 200, CIE = 100 and ESE = 100 marks

- Maximum grade (S grade) for the dissertation phase II will be awarded preferably if the student publishes the dissertation work in a peer reviewed journal.
- Final Evaluation (ESE) should be done by a three-member committee comprising of the Department Project coordinator, Guide and an External expert. The external expert shall be an academician or from industry.

(x) TEACHING ASSISTANCESHIP (TA)

All M.Tech students irrespective of their category of admission, shall undertakeTA duties for a minimum duration as per the curriculum. Being a TA, the student will get an excellent

opportunity to improve their expertise in the technical content of the course, enhance communication skills, obtain a hands-on experience in handling the experiments in the laboratory and improve peer interactions.The possible TA responsibilities include the following: facilitate a discussion section or tutorial for a theory/ course, facilitate to assist the students for a laboratorycourse, serve as a mentor for students, and act as the course webmaster. TAs may berequired to attend the instructor's lecture regularly. A TA shall not be employed as a substitute instructor, where the effect is to relieve the instructor of his or her teaching responsibilities.

For the tutorial session:

(i) Meet the teacher and understand your responsibilities well in advance, attend the lectures of the course for which you are a tutor, work out the solutionsfor all the tutorial problems yourself, approach the teacher if you find any discrepancy or if you need help in solving the tutorial problems, use reference text books, be innovative and express everything in English only.

(ii) Try to lead the students to the correct solutions by providing appropriatehints rather than solving the entire problem yourself, encourage questions fromthe students, lead the group to a discussion based on their questions, plan to askthem some questions be friendly and open with the students, simultaneously being firm with them.

(iii) Keep track of the progress of each student in your group, give a periodicfeedback to the student about his/her progress, issue warnings if the student is consistently under-performing, report to the faculty if you find that a particular student is consistently underperforming, pay special attention to slow-learnersand be open to the feedback and comments from the students and faculty.

(iv) After the tutorial session you may be required to grade the tutorials/assignments/tests. Make sure that you work out the solutions to the questions yourself, and compare it with the answer key, think and work out possible alternate solutions to the same question, understand the marking scheme from the teacher. Consult the teacher and make sure that you are not partial to some student/students while grading. Follow basic ethics.

Handling a laboratory Session:

(i) Meet the faculty – in- charge a few days in advance of the actual lab class and get the details of the experiment, get clarifications from him/her regarding all aspects of the experiment and the expectations, prepare by reading about the theoretical background of the experiment, know the physical concepts involved in the experiment, go to the laboratory and check out the condition of the equipment/instrumentation, perform the laboratory experiment at least onceone or two days before the actual laboratory class, familiarize with safety/ security aspects of the experiment / equipment/laboratory, prepare an instruction sheet for the experiment in consultation with the faculty, and keep sufficient copies ready for distribution to students for their reference.

(ii) Verify condition of the equipment/set up about 30 minutes before the students arrive in the class and be ready with the hand outs, make brief introductory remarks about the experiment, its importance, its relevance to thetheory they have studied in the class, ask the students suitable questions to know there level of preparation for the experiment, discuss how to interpret results, ask them comment on the results.

(iii) Correct/evaluate/grade the submitted reports after receiving suitable instructions from the faculty in charge, continue to interact with students if they have any clarifications regarding any aspect of the laboratory session, including of course grading, Carefully observe instrument and human safety in laboratory class, Preparing simple questions for short oral quizzing during explanation ofexperiments enables active participation of students, facilitate attention, provides feedback and formative evaluation.

POINTS TO REMEMBER

1. Arrange an awareness programme to all M.Tech students on day 1 regarding the curriculum and the regulation.
2. The departments should prepare the list of MOOC courses suitable to their programmes and encourage the students to complete at the earliest.
3. Make a tie up with industries by the middle of semester for Industry Integrated

Course. While choosing the course, it should be ensured that theprogramme is relevant and updated in that discipline. The Industry expert handling the course shall be a postgraduate degree holder. The evaluation procedure shall also be clearly explained to them.

4. Each department offering M.Tech programme should be careful in selectingthe mini project in semester 2.

5. The departments should invite the Industries/research organizations during first semester and inform them about the mandatory 6-8 weeks internship that the students should undergo after their second semester. Thepossibility of doing their dissertation at the Industry shall also be explored.They should also be made aware about the evaluation procedure of the Internships. They may also be informed that it is possible to continue internship provided if it leads to their dissertation. Proposals may becollected from them for allotting to students according to their fields of interest.

6. Make sure that all internal evaluations and the end semester examinations to be conducted by the college are carried out as per the evaluation procedure listed in the curriculum. Any dilution from the prescribed procedure shall be viewed seriously.

7. Teaching assistance shall be assigned to all students as per the curriculum. However, a TA shall not be employed as a substitute instructor,where the effect is to relieve the instructor of his or her teaching responsibilities.

8. The possible TA responsibilities include the following: facilitate a discussion section or tutorial for a theory/ course, facilitate to assist the students for a laboratory course, serve as a mentor for students, and act as the course web-master.

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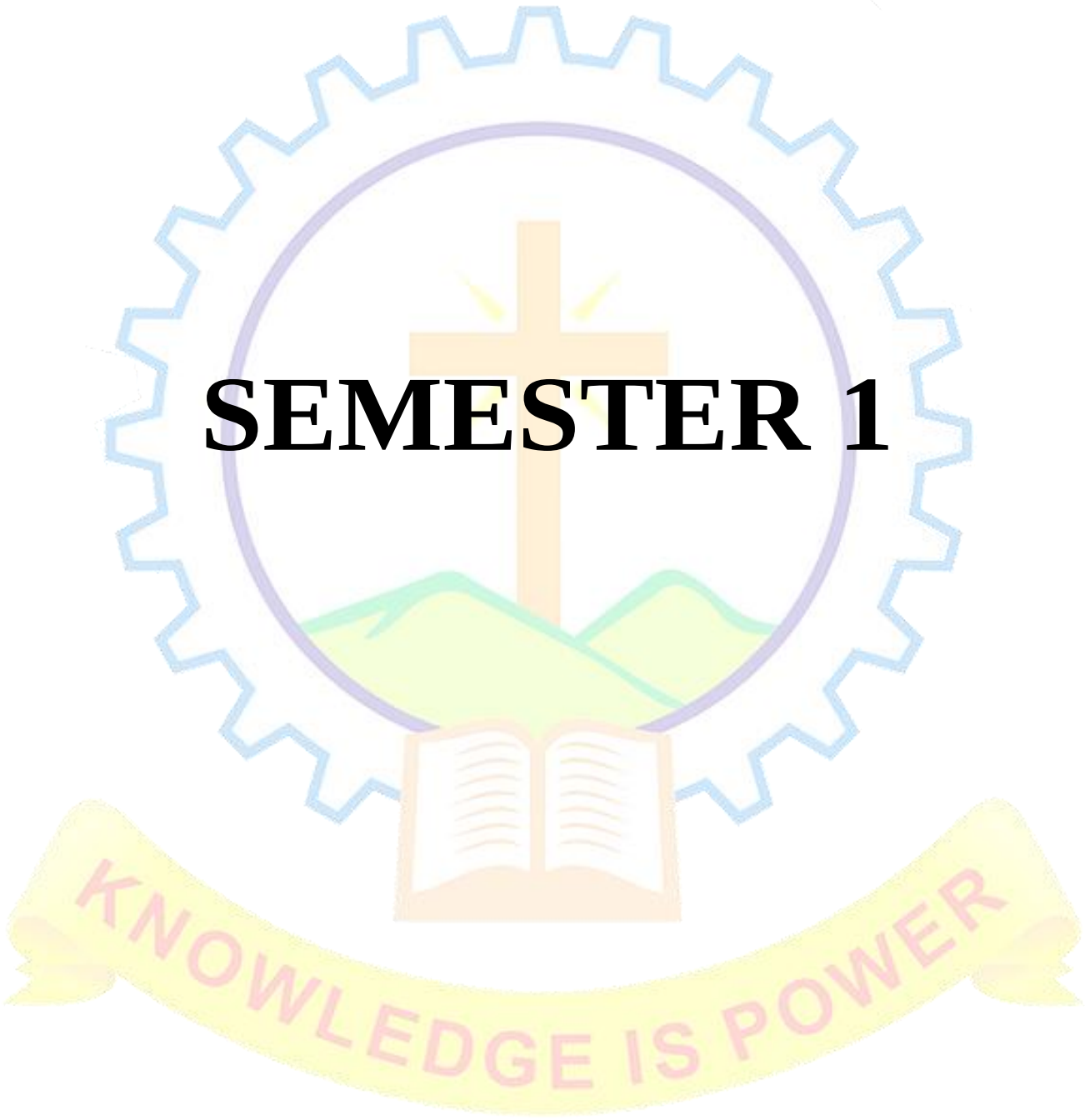


SEMESTER 1

Discipline: ELECTRONICS AND COMMUNICATION

Stream: VLSI AND EMBEDDED SYSTEMS

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1T101	Digital CMOS VLSI Design	Core	4	0	0	4	4

Preamble: This course aims to develop students a good knowledge of all aspects of Digital CMOS VLSI Design, its characteristics, designing and model various subsystems using CMOS logic.

Prerequisite: Solid State Devices, Basic MOS Transistor Theory

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design basic CMOS digital circuits and model the circuits to analyze the delay
CO 2	Understand interconnect, power analyses, I/O and clocking issues of CMOS Digital circuits
CO 3	Design various types of static and dynamic digital CMOS circuits
CO 4	Understand the timing concepts in latch and flip-flops.
CO 5	Design CMOS data path subsystems and memory arrays

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	2	2	3	3	2	2
CO 2	2	2	3	3	2	2
CO 3	2	2	2	3	2	2
CO 4	2	2	3	3	2	2
CO 5	2	2	3	3	2	2

Assessment Pattern

	Digital CMOS VLSI Design		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project	:10 marks
Course based task/Seminar/Quiz	:10 marks
Test paper 1 (Module 1 and Module 2)	:10 marks
Test paper 2 (Module 3 and Module 4)	:10 marks

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (9 hours)

Introduction to CMOS technology:

MOS Transistor Theory: IV and CV characteristics.
CMOS logic: NOT, NAND, NOR, Compound Logic, Pass transistor, Transmission gate, Tristate logic, Multiplexer.
Basics of CMOS fabrication and Layout: Fabrication Process, Layout Design Rules, Stick Diagrams, Design partitioning, Logic design, Circuit design, Physical design, Design verification, Fabrication, Packaging and testing.
Static CMOS Inverter: DC Characteristics, Beta Ratio Effects, Noise Margin, Pass Transistor DC Characteristics.

MODULE 2 (9 hours)

Delay Models: Introduction, Definitions, Timing Optimization.
RC Delay Model: Effective Resistance, Gate and Diffusion Capacitance, Equivalent RC Circuits, Elmore Delay, Layout Dependence of Capacitance, Determining Effective Resistance.
Linear Delay Model: Logical Effort, Parasitic Delay, Delay in a Logic Gate.
Logical Effort of Paths: Delay in Multistage Logic Networks, Choosing the Best Number of Stages.

MODULE 3 (9 hours)

Interconnect effects and power analysis: Introduction, Wire Geometry and Interconnect Modelling: Resistance, Capacitance, and Inductance.
Interconnect Impact: Delay, Energy, Crosstalk, Inductive Effects, Effective Resistance and Elmore Delay.
Power: Sources of Power Dissipation, Dynamic Power, Static Power, On-Chip Power Distribution

Network. On-Chip Bypass Capacitance, Power Network Modelling , Power Supply Filtering, Charge Pumps. Energy Scavenging.

Clocks: Clock System Architecture, Global Clock Generation, Global Clock Distribution, Local Clock Gaters. PLLs and DLLs.

I/O: Basic I/O Pad Circuits, Electrostatic Discharge Protection.

MODULE 4 **(9 hours)**

Combinational Circuit Design

Static CMOS circuits: Ratioed Circuits, CMOS Inverter, tristate inverter, Other static CMOS logic gates, static properties (2 input NAND, NOR), Combinational logic circuits.

Fundamentals of dynamic logic: Dynamic pass transistor circuits, CMOS circuits, High performance dynamic circuits-Domino CMOS, Multi Output Domino Logic, NP Domino logic (NORA),

BiCMOS: NOT, NAND and NOR

FF and Latches: True-Single-Phase-Clock (TSPC) CMOS logic.

Silicon-On-Insulator Circuit Design: Floating Body Voltage, SOI Advantages, Disadvantages.

Introduction to System on chip (SOC).

Introduction to Network on chip (NOC).

MODULE 5 (9 hours)

Data path Subsystems:

Adders: Single-Bit Addition, Carry-Propagate Addition, Subtraction, Multiple-Input Addition

Multipliers: Unsigned Array Multiplication, Booth Encoding, Column Addition, Final Addition.

Shifters: Funnel Shifter, Barrel Shifter.

Comparators: Magnitude Comparator.

Counters: Binary Counters.

Designing of memory and array structures: SRAM, DRAM, and Embedded DRAM. Read-Only Memory, Content-Addressable Memory, Programmable Logic Arrays.

.

Reference Books

1. Weste and Harris, CMOS VLSI Design A Circuits and Systems Perspective, 4/E, Pearson
2. Weste and Harris, “Integrated Circuit Design”, 4/e, 2011, Pearson Education**.**
3. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits, 3/e, Tata McGraw-Hill Education, 2003.
4. Rabaey, Chandrakasan and Nikolic, “Digital Integrated Circuits – A Design Perspective”, 2/e, Pearson Education.
5. R. Jacob Baker, Harry W. Li, David E. Boyce, “CMOS, Circuit Design, Layout, and Simulation”, 3/e, Wiley Interscience.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	**MOS Transistor Theory**: IV and CV characteristics.	1
1.2	**CMOS logic**: NOT, NAND, NOR, Compound Logic, Pass transistor, Transmission gate, Tristate logic, Multiplexer.	2
1.3	**Basics of CMOS fabrication and Layout**: Fabrication Process, Layout Design Rules, Stick Diagrams, Design partitioning, Logic design, Circuit design, Physical design, Design verification, Fabrication, Packaging and testing.	3
1.4	**Static CMOS Inverter**: DC Characteristics, Beta Ratio Effects, Noise Margin.	2
1.5	Pass Transistor DC Characteristics	1
	Module 2	
2.1	**Delay Models**: Introduction, Definitions, Timing Optimization.	1
2.2	**RC Delay Model**: Effective Resistance, Gate and Diffusion Capacitance, Equivalent RC Circuits, Elmore Delay, Layout Dependence of Capacitance, Determining Effective Resistance.	3
2.3	**Linear Delay Model**: Logical Effort, Parasitic Delay, Delay in a Logic Gate.	3
2.4	**Logical Effort of Paths:** Delay in Multistage Logic Networks, Choosing the Best Number of Stages.	2
	Module 3	
3.1	**Interconnect effects and power analysis**: Introduction, Wire Geometry and Interconnect Modelling: Resistance, Capacitance, and Inductance.	2
3.2	**Interconnect Impact**: Delay, Energy, Crosstalk, Inductive Effects, Effective Resistance and Elmore Delay.	2
3.3	**Power:** Sources of Power Dissipation, Dynamic Power, Static Power, On-Chip Power Distribution Network. On-Chip Bypass Capacitance, Power Network Modelling , Power Supply Filtering, Charge Pumps. Energy Scavenging.	2
3.4	**Clocks:** Clock System Architecture, Global Clock Generation, Global Clock Distribution, Local Clock Gaters. PLLs and DLLs.	2
3.5	**I/O**: Basic I/O Pad Circuits, Electrostatic Discharge Protection.	1
	Module 4	
4.1	**Static CMOS circuits:** Ratioed Circuits, CMOS Inverter, tristate inverter, Other static CMOS logic gates, static properties (2 input NAND, NOR), Combinational logic	3

	circuits.	
4.2	**Fundamentals of dynamic logic**: Dynamic pass transistor circuits, CMOS circuits, High performance dynamic circuits-Domino CMOS, Multi Output Domino Logic, NP Domino logic (NORA)	2
4.3	**BiCMOS**: NOT, NAND and NOR	1
4.4	FF and Latches: True-Single-Phase-Clock (TSPC) CMOS logic	1
4.5	**Silicon-On-Insulator Circuit Design:** Floating Body Voltage, SOI Advantages, Disadvantages	1
4.6	**Introduction to System on chip (SOC). Introduction to Network on chip (NOC).**	1
	Module 5	
5.1	**Adders:** Single-Bit Addition, Carry-Propagate Addition, Subtraction, Multiple-Input Addition	2
5.2	**Multipliers:** Unsigned Array Multiplication, Booth Encoding, Column Addition, Final Addition.	2
5.3	**Shifters:** Funnel Shifter, Barrel Shifter.	1
5.4	**Comparators:** Magnitude Comparator.	1
5.5	**Counters:** Binary Counters	1
5.6	**Designing of memory and array structures:** SRAM, DRAM, and Embedded DRAM. Read-Only Memory, Content-Addressable Memory, Programmable Logic Arrays	2

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: M24EC1T101

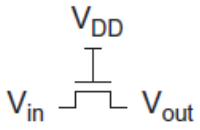
Course Name: Digital CMOS VLSI Design

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Suppose *VDD* = 3.2 V and *Vt* = 0.4 V. Determine *V*out for the following circuit. Neglect the body effect.



*V*in = 0 V
*V*in = 0.6 V
*V*in = 0.9 V
*V*in = 3.2 V.

2. Model an nMOS transistor with width equal to 2. Draw the equivalent circuit.
3. What is electrostatic discharge protection? Draw the circuit for the same.
4. Describe the tristate CMOS inverter.
5. Illustrate how a subtraction can be implemented using adder.

PART B

Answer any five questions. Each question carries 8 marks.

6. a. Design a static CMOS inverter with equal rise and fall resistance. What is the effect of beta ratio in the working of inverter? (4 marks)

b. Draw the cross-sectional view of the fabrication procedure involved in a CMOS inverter. Draw the stick encoding of the CMOS inverter. (4 marks)

7. a. Sketch a transistor-level schematic for a CMOS 4-input NOR gate. Find out the width of transistors to achieve unit rise and fall resistance. (4 marks)

b. Design an unit inverter driving 4 identical unit inverter. Draw the RC model and find out the propagation delay. R=10K and C=0.1Pf. (4 marks)

8. a. A unit inverter is driving 4 unit inverter at the end of a 1mm long, 0.32µm wide wire in a 180nm

process. The sheet resistance is 0.05ohms/square and the capacitance is 0.2fF/μm. Find the Elmore delay by constructing a π model for the wire. Resistance of unit nMOS is 10KΩ and gate capacitance is 0.1pF. (4 marks)

b How crosstalk affects the data transmission in an interconnect wire. What are the different methods of cross- talk control? (4 marks)

9. a. Design a dynamic CMOS inverter cascaded with another dynamic inverter. Draw the timing diagram and explain the monotonicity problem. How we can eliminate this problem. (4 marks)

b. Design a 3-input BiCMOS NAND gate. Label the transistor widths. What is the logical effort? (4 marks)

10. a. With proper timing diagram explain the working of NP Domino logic. (4 marks)

b. Sketch a transistor level schematic of the following functions:

(i) Y=(A+B).C+D.E

(ii) Y=(A+B).(C+D) (4 marks)

11. a. With proper schematics explain the how a PG carry ripple adder is implemented. (4 marks)

b. Sketch and explain the working principle of a 4 bit barrel shifter. (4 marks)

12. a. Design a carry skip adder and explain. (4 marks)

b. Explain with example a RADIX 4 booth encoding multiplier. (4 marks)

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1T102	FPGA BASED SYSTEM DESIGN	Core	4	0	0	4	4

Preamble: The purpose of this course is to introduce basic concepts of FPGA based system design and to impart practical skills in developing a synthesizable digital sub system using Verilog HDL.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply Verilog programming to develop and simulate digital sub systems. (Cognitive Knowledge Level: Apply)
CO 2	Design RT-level combinational and regular sequential circuits (Cognitive Knowledge Level: Create)
CO 3	Construct FSM and FSMD (Cognitive Knowledge Level: Analyse)
CO 4	Analyse and implement UART subsystems in FPGA (Cognitive Knowledge Level: Evaluate)
CO 5	Explain architecture and features of programmable logic devices (Cognitive Knowledge Level: Analyse)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	2		3	2	2	1
CO 2	3		3	3	2	1
CO 3	1		2	3	2	1
CO 4			2	3	2	1
CO 5	2		3	3	3	1

Assessment Pattern

Bloom's Category	FPGA BASED SYSTEM DESIGN		
	Continuous Internal Evaluation		End Semester Examination (% Marks)
	Test 1 (% Marks)	Test 2 (%Marks)	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project :10 marks

Course based task/Seminar/Quiz :10 marks

Test paper 1 (Module 1 and Module 2) :10 marks

Test paper 2 (Module 3 and Module 4) :10 marks

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (9 hours)

Verilog HDL – based design, Overview of FPGA and EDA software: Introduction, General description, Basic lexical elements and data types, Data types, Program skeleton, Structural description, Gate-level combinational circuit, Testbench, Introduction and overview of a general FPGA device, Gate-level greater-than circuit, Gate-level binary decoder.

MODULE 2 (9 hours)

RT-level combinational circuit and Regular sequential circuit: Introduction, Operators, Always block for a combinational circuit, if statement, Case statement, General coding guidelines for an always block, Parameter and constant, Design examples: shift register, Binary counters, Introduction to Regular Sequential Circuit, HDL code of the FF and register, Test bench for sequential circuits, Case study.

MODULE 3 (9 hours)

FSM: Introduction, FSM representation and code development, Mealy and Moore outputs, Design examples. FSMD-Introduction, ASMD chart, Code development of an FSMD, Design examples.

MODULE 4 (9 hours)

Implementation of UART sub system: Introduction, UART receiving subsystem, UART transmitting subsystem, Overall UART system, Full-featured UART, UART with an automatic baud rate detection circuit, UART with an automatic baud rate and parity detection circuit, UART-controlled stopwatch, UART-controlled rotating LED banner.

MODULE 5 (9 hours)

VGA controller: Basic operation of a CRT, Video controller, VGA synchronization, Horizontal synchronization, Vertical synchronization, Timing calculation of VGA synchronization signals, HDL implementation, Testing circuit, Overview of the pixel generation circuit, Graphic generation with an object-mapped scheme, rectangular objects, non-rectangular object, Animated object, Graphic generation with a bit-mapped scheme.

Reference Books

1. Pong P. Chu, "FPGA Prototyping by Verilog Examples", John Wiley & Sons, 2008
2. FPGA-Based System Design – Wayne Wolf, Verlag: Prentice Hall
3. Modern VLSI Design: System-on-Chip Design (3rdEdition) Wayne Wolf, Verlag
4. Field Programmable Gate Array Technology- S. Trimberger, Edr, 1994, Kluwer Academic
5. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, 1994, Prentice Hall
6. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Second Edition, Prentice Hall PTR, 2003
7. B. Bala Tripura Sundari, T. R. Padmanabhan, "Design Through Verilog HDL", Wiley India, 2012

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Verilog HDL – based design, Overview of FPGA and EDA software: Introduction	1
1.2	General description, Basic lexical elements and data types, Data types	2
1.3	Program skeleton, Structural description	1
1.4	Gate-level combinational circuit, Testbench	2
1.5	Introduction and overview of a general FPGA device	1
1.6	Gate-level greater-than circuit	1
1.7	Gate-level binary decoder	1
	Module 2	
2.1	RT-level combinational circuit and Regular sequential circuit: Introduction	1
2.2	Operators, always block for a combinational circuit	1
2.3	If statement, Case statement	1
2.4	General coding guidelines for an always block, Parameter and constant	1

2.5	Design examples: shift register, Binary counters	1
2.6	Introduction to Regular Sequential Circuit	1
2.7	HDL code of the FF and register, Test bench for sequential circuits	1
2.8	Case study	2
	Module 3	
3.1	FSM: Introduction, FSM representation and code development	1
3.2	Mealy and Moore outputs	1
3.3	Design examples	2
3.4	FSMD-Introduction	1
3.5	ASMD chart	1
3.6	Code development of an FSMD	1
3.7	Design examples	2
	Module 4	
4.1	Implementation of UART sub system: Introduction	1
4.2	UART receiving subsystem	1
4.3	UART transmitting subsystem	1
4.4	Overall UART system	1
4.5	Full-featured UART	1
4.6	UART with an automatic baud rate detection circuit	1
4.7	UART with an automatic baud rate and parity detection circuit	1
4.8	UART-controlled stopwatch	1
4.9	UART-controlled rotating LED banner	1
	Module 5	
5.1	VGA controller: Basic operation of a CRT, Video controller	1
5.2	VGA synchronization, Horizontal synchronization, Vertical synchronization	2
5.3	Timing calculation of VGA synchronization signals, HDL implementation	1
5.4	Testing circuit, Overview of the pixel generation circuit	1
5.5	Graphic generation with an object-mapped scheme, rectangular objects, non-rectangular object,	2
5.6	Animated object, Graphic generation with a bit-mapped scheme	2

CO ASSESSMENT QUESTIONS Course Outcome 1 (CO1):

1. Solve problems on combinational circuits.
2. Design test benches for combinational circuits.
3. Design gate level circuits

Course Outcome 2 (CO2):

1. Design RT Level circuits.
2. Design HDL code for sequential circuits.

3. Design test benches for sequential circuits.

Course Outcome 3 (CO3):

1. Design Mealy and Moore machines.
2. Develop FSMD and ASM charts.
3. Develop test benches for state machines.

Course Outcome 4 (CO4):

1. Demonstrate UART transmitter using FPGA board.
2. Demonstrate UART receiver using FPGA board.
3. Develop a UART controlled stop watch.

Course Outcome 5 (CO5):

1. Design and demonstrate a VGA controller to display a filled circle on VGA display.
2. Design and demonstrate a VGA controller to display a filled rectangle on VGA display.
3. Design and demonstrate a VGA controller to display a moving line on VGA display.

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: M24EC1T102

Course Name: FPGA BASED SYSTEM DESIGN

Max. Marks: 60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Write Verilog code for 2 bit Gate-level greater than circuit.
2. Design a 2 bit priority encoder.
3. Design a Moore based rising edge detector
4. Draw the conceptual block diagram of a UART receiving subsystem.
5. Draw the timing diagrams for a 640 x 480 VGA screen with a 25MHz Pixel rate.

PART B

Answer any five questions. Each question carries 8 marks.

6. Write a Verilog code for N-bit free running shift register.
7. Design a Fibonacci number circuit using Verilog.
8. Design a stopwatch which displays the time in three decimal digits and counts from 00.0 to 99.9 seconds and wraps.
9. Design a UART receiver with 9600 baud rate and 25MHZ clock using Verilog.
10. Design a VGA system to display a circle at the center of the screen.
11. Design a debouncing circuit with RT methodology.
12. Design a VGA system to display a line from the left top corner to the right bottom corner.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1T103	Design With Advanced Microcontroller	Program Core	4	0	0	4	4

Preamble: To allow students in Embedded System sectors to learn programming / Interfacing peripherals to ARM Cortex based Microcontroller

Prerequisite: Knowledge of basic microcontrollers like 8051 and microcontroller programming using assembly language program and Embedded C.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Gain Knowledge about the architectural features and instructions of 32 bit ARM Cortex M3 microcontroller.
CO 2	Understand the selection of programming language and embedded C
CO 3	Understand the basic hardware components and their selection method based on the characteristics and attributes of an Embedded System.
CO 4	Understand various Sensors, Actuators & Interfacing Modules.
CO 5	Students must be able to design and implement an embedded system to meet the requirements of real time application.

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineeringfraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the speCIElization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyse and solve practical engineering problems.
PO 6	An ability to engage in life-long learning for the design and development of the stream related problems taking into consideration sustainability, societal, ethical and environmental aspects. Also to develop cognitive skills for project management and finance which focus on Industry and Entrepreneurship.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1		1	2	2	2
CO 2	1		1	2	2	2
CO 3	1		1	2	2	2
CO 4	2		1	2	2	3
CO 5	3	1	1	2	2	3

Assessment Pattern

	M24EC1T103 - Design With Advanced Microcontroller		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	**CIE marks**	**ESE marks**	**ESE Duration**
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project : 10 marks

Course based task/Seminar/Quiz : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of theexamination will be 3 Hrs.

SYLLABUS

MODULE 1: **ARM-32 bit MICROCONTROLLER (7 Hrs)**

Getting familiar with Embedded Systems. ARM Design Philosophy & RISC Architecture, Programmer's Model. ARM Cortex M, Cortex M Architecture, ARM Cortex-M Internals & Debugging.

MODULE 2: **GPIO MANAGEMENT (7 Hrs)**

GPIO Configuration, Driving De-initialization, Interfacing IO devices and its type – LEDs, Switches, Buzzer, Seven Segment Display, LCD (4 bit, 8 bit Mode), Keypad (4*4), DC Motor, Stepper Motor, Servo motor, Relay.

MODULE 3: **INTERRUPT MANAGEMENT & UART (7 Hrs)**

NVIC Controller, Enabling Interrupt, Interrupt Priority Levels, UART Initialization, UART communication in polling Mode & in Interrupt Mode.

MODULE 4 : PWM, TIMERS , ADC, & DAC (7 Hrs)

Timers Basics, General Purpose Timer, SysTick Timer, ADC & DAC Basics, Initialization, DAC Peripherals & Modules. Analog Sensors and its Types(Ultrasonic Sensor, Temperature, Humidity, Soil Moisture Sensor, PIR sensor)

MODULE 5 : I2C, SPI, CAN (8 Hrs)

I2C specification, Protocol configuration, I2C Peripherals.
SPI Specification, Protocol configuration, it's Peripheral and Modules.
CAN Protocols Overview, Application, Architecture, Data Transmission & Data Frames.

Reference Books

1. Shibu K V —Introduction to Embedded Systems, Tata McGraw Hill Education Private Limited, 2nd Edition
2. Noviello, Carmine. "Mastering STM32."
3. Norris, Donald. Programming with STM32: Getting Started with the Nucleo Board and C/C++. McGraw Hill Professional, 2018.
4. STM32F10xx User Manual

COURSE CONTENTS AND LECTURE SCHEDULE

(For 4 credit courses, the content can be for 45 hrs. and for 3 credit courses, the content can be for 36 hrs.)

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Getting familiar with Embedded Systems	1
1.2	ARM Design Philosophy & RISC Architecture	1
1.3	Programmer's Model	1
1.4	ARM Cortex M	1
1.5	Cortex M Architecture	1
1.6	ARM Cortex-M Internals & Debugging	1
	Module 2	
2.1	GPIO Configuration, Driving De-initialization,	1
2.2	Interfacing IO devices and its type	1
2.3	LEDs, Switches, Buzzer interface	1
2.4	Seven Segment Display interface	1
2.5	LCD (4 bit, 8 bit Mode) interface	1
2.6	Keypad (4*4) interface	1
2.7	DC Motor, Stepper Motor, Servo motor -interface	2
2.8	Relay interface	1
	Module 3	
3.1	NVIC Controller	1
3.2	Enabling Interrupt	1
3.3	Interrupt Priority Levels	1
3.4	UART Initialization	1
3.5	UART communication in polling Mode & in Interrupt Mode.	2
	Module 4	
4.1	Timers Basics	1
4.2	General Purpose Timer	1
4.3	SysTick Timer	1
4.4	ADC & DAC Basics, Initialization	2
4.5	DAC Peripherals & Modules	1
4.6	Analog Sensors and its Types	1
4.7	Ultrasonic Sensor, Temperature, Humidity, Soil Moisture Sensor, PIR sensor	3
	Module 5	
5.1	I2C specification, Protocol configuration, I2C Peripherals	3
5.2	SPI Specification, Protocol configuration, it's Peripheral and Modules	3
5.3	CAN Protocols Overview, Application, Architecture, Data Transmission & Data Frames.	3

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: M24EC1T103

Course Name: **Design with Advanced Microcontroller**

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

13. What are the major features of RISC architecture? How the ARM processor is different from pure RISC architecture?

14. What are the various stages of 5-stage pipelining in ARM 9 processor?

15. Which are the 37 registers of ARM processor? How the registers are organised?

16. Illustrate how the interrupts are multiplexed in the TMS320F28335 processor. External interrupts and PIE interrupt sources must accounted and the interrupt multiplexing must be represented using appropriate diagrams.

17. What are the configuration steps used for the GPIO pins of the TMS320F28335 processor?

(4x5=20 Marks)

PART B

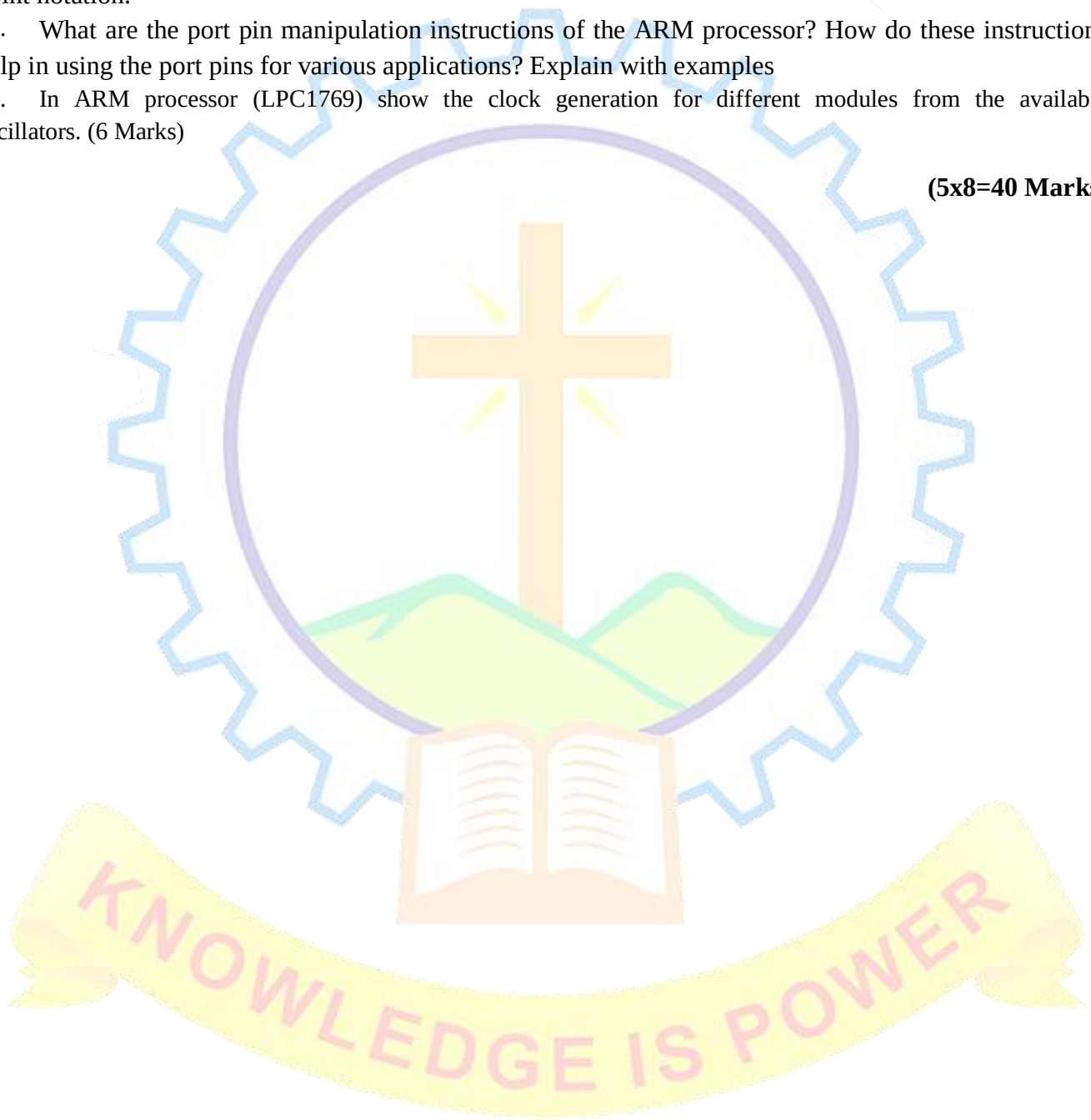
Answer any five questions. Each question carries 8 marks.

6. Draw and explain LPC1769 clock generation block diagram.

7. Write instructions to copy a block of memory (128 bytes aligned) if r9 indicates the address of the source, r10 indicates the address of the destination and r11 indicates the end address of the source.

8. Differentiate AHB, ASB and APB in advanced microcontroller bus architecture.
9. Explain the most widely used industrial serial communication protocol available in LPC1769 microcontroller.
10. Write the number 2005 in 32-bit binary, binary coded decimal, ASCII and single precision floating point notation.
11. What are the port pin manipulation instructions of the ARM processor? How do these instructions help in using the port pins for various applications? Explain with examples
12. In ARM processor (LPC1769) show the clock generation for different modules from the available oscillators. (6 Marks)

(5x8=40 Marks)



SEMESTER I
PROGRAM ELECTIVE I

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E104A	PHYSICAL DESIGN AUTOMATION	PROGRAM ELECTIVE 1	3	0	0	3	3

Preamble: This course aims to familiarize various stages of VLSI Physical Design and algorithms used to automate the process.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply Search Algorithms and Shortest Path Algorithms to graphs representing VLSI problem formulations
CO 2	Outline VLSI Design Flow, Design Styles and Apply Partitioning Algorithms to graphs representation of circuits
CO 3	Illustrate Layout Design Rules and Apply different algorithms for layout compaction
CO 4	Make use of different concepts in Floor plan, Placement and Pin Assignment to Apply suitable algorithms for finding solutions
CO 5	Understand Routing strategies and Apply algorithms to solve Routing requirements.

Mapping of course outcomes with program outcomes

	PO1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2	3	4		
CO 2	1	2	3	4		
CO 3	1	2	3	4		1
CO 4	1	2	3	4	5	1
CO 5	1	2	3	4	5	

Assessment Pattern

Course name	PHYSICAL DESIGN AUTOMATION		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar*	: 10 marks
Course based task/Micro Project//Data collection and interpretation/Case study	: 10 marks
Test paper 1 (Module 1 and Module 2)	: 10 marks
Test paper 2 (Module 3 and Module 4)	: 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 Graph Terminology, Search Algorithms and Shortest Path Algorithms (8 hours)

Basic graph theory terminology, Data structures for representation of Graphs – Adjacency Matrix, Adjacency List, Breadth First Search, Depth First Search, Topological Sort, Breadth First Search, Depth First Search, Topological Sort, Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path, Prim's Algorithm for Minimum Spanning Tree.

MODULE 2 Design Automation and Partitioning Algorithms (9 hours)

VLSI Design Flow, Physical Design Flow, VLSI Design Styles, Terminology, Optimization Goals, Levels of Partitioning, Parameters for Partitioning, Kernighan-Lin Algorithm, FiducCIE-Mattheyses Algorithm

MODULE 3 Layout Compaction (8 hours)

Layout Layers and Design Rules, Physical Design Optimizations, Applications of Compaction, Graph Theoretical Formulation, Maximum Distance Constraints, Longest Path Algorithm for DAGs, Longest Path in Graph with Cycles - Liao-Wong Algorithm

MODULE 4 Floor planning, Placement and Pin Assignment (8 hours)

Optimization Goals, Slicing Floorplan, Non-Slicing Floorplan, Constraint Graphs, Conversion of Floorplan to a Constraint Graph Pair, Floorplan Sizing, Shape Functions, Corner Points, Minimum Area Algorithm,

Optimization Objectives, Wirelength Estimation, Weighted Wirelength, Maximum Cut Size, Wire Density, Concentric Circle Method, Topological Pin Assignment

MODULE 5 Routing (7 hours)

Terminology and Definitions, Optimization Goals, Representation of Routing Regions, Area Routing, Lee's Algorithm, Hadlock Algorithm, Channel Routing, Horizontal and Vertical Constraint Graph, Left-Edge algorithm

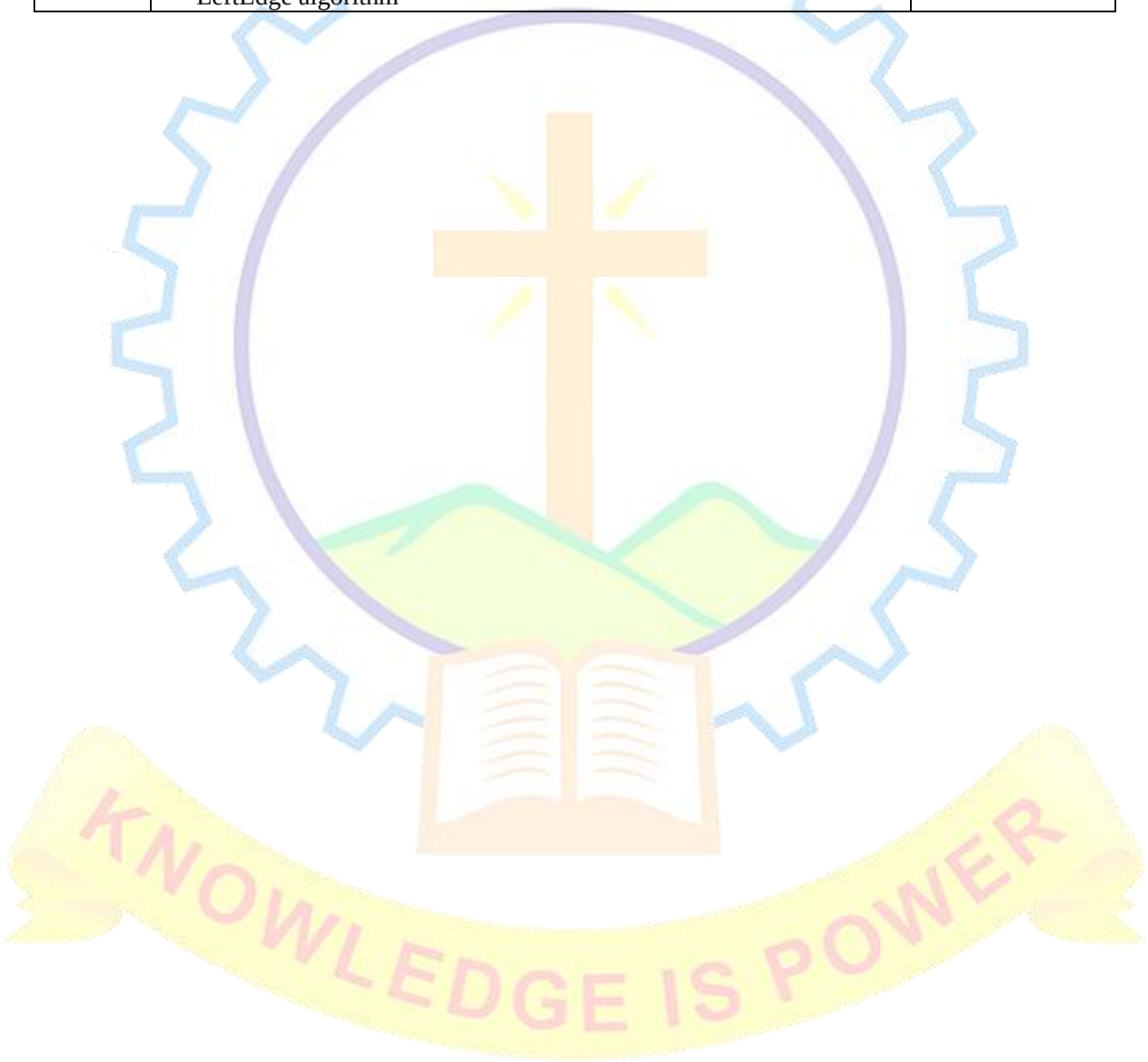
Text Books

1. Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2011th edition.
2. Gerez,Sabih H., "Algorithms for VLSI Design Automation", John Wiley & Sons, 2006.
3. Sherwani, Naveed A., "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 1999.
4. Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest. "Introduction to Algorithms." The MIT Press, 3rd edition, 2009.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1 Graph Terminology, Search Algorithms and Shortest Path Algorithms	
1.1	Basic graph theory terminology, Data structures for representation of Graphs – Adjacency Matrix, Adjacency List	2
1.2	Breadth First Search, Depth First Search, Topological Sort	3
1.3	Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path, Prim's Algorithm for Minimum Spanning Tree	3
	Module 2 Design Automation and Partitioning Algorithms	
2.1	VLSI Design Flow, Physical Design Flow, VLSI Design Styles	3
2.2	Terminology, Optimization Goals, Levels of Partitioning, Parameters for Partitioning	2
2.3	Kernighan-Lin Algorithm, FiducCIE-Mattheyses Algorithm	4
	Module 3 Layout Compaction	
3.1	Layout Layers and Design Rules, Physical Design Optimizations	2
3.2	Applications of Compaction, Graph Theoretical Formulation, Maximum Distance Constraints	2
3.3	Longest Path Algorithm for DAGs, Longest Path in Graph with Cycles -Liao-Wong Algorithm	4
	Module 4 Floorplanning, Placement and Pin Assignment	
4.1	Optimization Goals, Slicing Floorplan, Non-Slicing Floorplan, Constraint Graphs, Conversion of Floorplan to a Constraint Graph Pair	3
4.2	Floorplan Sizing, Shape Functions, Corner Points, Minimum	3

	Area Algorithm	
4.3	Optimization Objectives, Wirelength Estimation, Weighted Wirelength, Maximum Cut Size, Wire Density	1
4.4	Concentric Circle Method, Topological Pin Assignmen	1
	Module 5 Routing	
5.1	Terminology and Definitions, Optimization Goals, Representation of Routing Regions	1
5.2	Area Routing, Lee's Algorithm, Hadlock Algorithm	3
5.3	Channel Routing, Horizontal and Vertical Constraint Graph, LeftEdge algorithm	3



Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E104A**

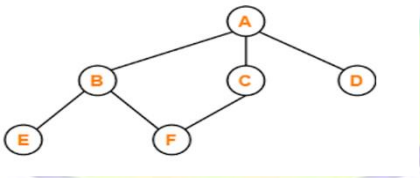
Course Name: Physical Design Automation

Max. Marks:60 Duration: 3 hours

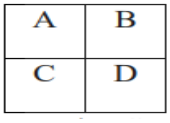
PART A

Answer all questions. Each question carries 4 marks.

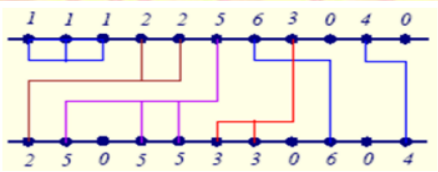
1. Perform topological sorting on the following graph.



2. KL algorithm is an example of a balanced partitioning algorithm. Justify.
3. Can longest path algorithm for directed acyclic graphs (DAG) be used as an alternate for shortest path algorithm? If yes, suggest at least two modifications.



4. Consider the floorplan given below, consisting of fourleaf cells: A, B, C and D. Draw two slicing tree representations.
5. For the following Channel Routing problem, what is the channel density?

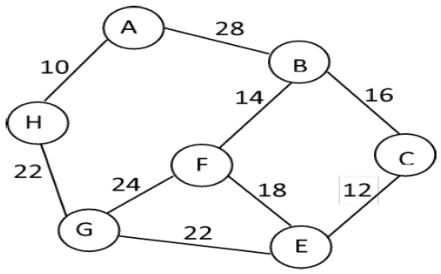


Pages: 2

PART B

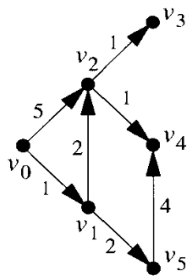
Answer any five questions. Each question carries 8 marks.

6. Apply Dijkstra's Algorithm on the graph shown below to find shortest path to all vertices from the vertex H.

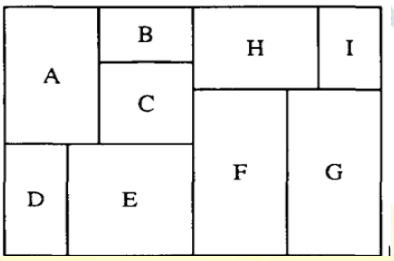


7. Draw the flowchart for VLSI Physical Design cycle.

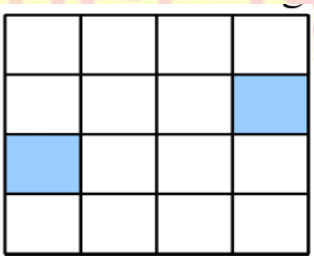
8. Apply Longest Path Algorithm to the following graph to find the longest path from V0.



9. Draw the Vertical and Horizontal Constraint Graph for the following floorplan.

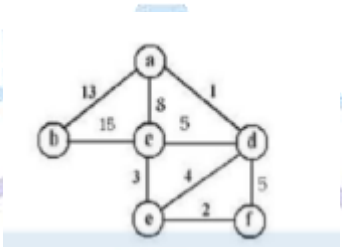


10.

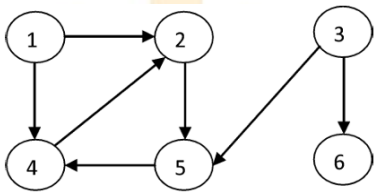


11. Apply Prim's algorithm to find the minimum spanning tree of the graph shown below.

Pages: 3



12. Consider the graph G(V, E) shown below. Assume 1 is the starting node.



Perform Depth First Search and Breadth First Search on the above graph.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E104B	EDA TOOLS	PROGRAM ELECTIVE 1	3	0	0	3	3

Preamble: 1. To understand the basic methodology of Digital and Analog system design.
2. To know the EDA tool concepts used for electronic system design for ICs.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply the design methodology of EDA for Digital Simulation
CO 2	Analyse the Synthesis steps of Digital circuits for optimal performance
CO 3	Evaluate the architectures for testing and testability of Digital circuits
CO 4	Evaluate the libraries for Digital circuits, create the layouts for the circuits and evaluate the verification method
CO 5	Analyse the analog and mixed signal simulation methods

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1		2	3	4	5	
CO 2		2	3	4	5	
CO 3			3	4		
CO 4			3	4		
CO 5		2	3	4	5	

Assessment Pattern

Course name	EDA TOOLS		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Concepts of EDA: Design Methodology Development steps - algorithmic model, register transfer level, logic design, transistor level circuit design, polygon pushing, design for test Implementation flow Top down vs Bottom up design process Application specific integrated circuits – design goals, design styles Design Libraries - Digital libraries, Pad cell Libraries, Analogue libraries, Macro Libraries.

MODULE 2 (8 hours)

Simulations:

Digital Simulation: Why?, Simulation Model, SDF, Structure of a Digital Simulator, Fault simulation, Performance & Use of logic simulation, Verification of Testability with Simulation, Limits of Digital Simulation.

Analog Simulation: Spice concept, Spice transistor models, Models of Operational Amplifiers, Analysis of Loop gain as Stability Criterion of Analog Circuits.

Mixed Signal Simulation: Overview, Simulation on different levels of abstraction, Concept of Mixed signal simulators.

MODULE 3 (9 hours)

Design for Testability Fundamentals: Faults in Digital circuits and their modeling, Fault simulation and fault collapsing, Digital test pattern generation–ATPG, ATPG algorithms, ATPGVector Formats and Compaction and Compression. Scan Architectures- Testability, Scan Registers, Generic scan based designs, Boundary Scan-JTAG. Built in Self Test (BIST) - BIST concepts and test pattern generation Test pattern generation for Combinational Circuits Test pattern for Sequential Circuits.

MODULE 4 (8 hours)

Synthesis and Formal Verification: Synthesis - Introduction, Examples, Partitioning, Modification of Hierarchy, Optimization, Retiming, Technology mapping. Formal Verification: Model checking, Equivalence checking, Fundamental techniques, Sequential circuits, Correctness of Synthesis steps, Design verification.

MODULE 5 (7 hours)

Geometric Layout and Geometric Verification: Layout of CMOS circuits: layers in CMOS layout, latch-up speCIEl requirements for analog layout, substrate noise Devices in CMOS : resistors, capacitors, diodes, BJT; Data formats: LEF Data format, GDSII Data format Standard cell Layout: standard cells, abstract view, floor planning, placement, routing Geometric Verification: Introduction, Layer preprocessing, Design Rule check, Extract, Extraction of parasitic capacitors and resistors, ERC, LVS.

Reference Books

1. Jansen, Dirk,"The Electronic Design Automation Handbook", 2003.
2. MironAbramovici, Melvin A.Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
3. M.J.S.Smith.,"Application-Specific Integrated Circuits", Addison Wesley.
4. Jan M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits- a Design perspective", Pearson education/ Prentice-Hall India Ltd, 2nd edition.
5. M.H.Rashid,"SPICE FOR Circuits And Electronics Using PSPICE", Prentice Hall, 2nd edition

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1 : Concepts of EDA	
1.1	Design Methodology Development steps - algorithmic model, register transfer level, logic design, transistor level circuit design, polygon pushing, design for test	2
1.2	Implementation flow Top down vs Bottom up design process	2
1.3	Application specific integrated circuits – design goals, design styles	2

1.4	Design Libraries - Digital libraries, Pad cell Libraries, Analogue libraries, Macro Libraries	2
	Module 2 : Simulations	
2.1	Digital Simulation :Why?, Simulation Model, SDF, Structure of a Digital Simulator, Fault simulation, Performance & Use of logic simulation, Verification of Testability with Simulation, Limits of Digital Simulation.	3
2.2	Analog Simulation: Spice concept, Spice transistor models, Models of Operational Amplifiers, Analysis of Loop gain as Stability Criterion of Analog Circuits.	3
2.3	Mixed Signal Simulation: Overview, Simulation on different levels of abstraction, Concept of Mixed signal simulators	2
	Module 3 : Design for Testability Fundamentals	
3.1	Faults in Digital circuits and their modeling, Fault simulation and fault collapsing,	2
3.2	Digital test pattern generation–ATPG, ATPG algorithms, ATPGVector Formats and Compaction and Compression.	2
3.3	Scan Architectures- Testability, Scan Registers, Generic scan based designs, Boundary Scan-JTAG.	2
3.4	Built in Self Test (BIST) - BIST concepts and test pattern generation	2
3.5	Test pattern generation for Combinational Circuits Test pattern for Sequential Circuits	1
	Module 4 : Synthesis and Formal Verification	
4.1	Synthesis - Introduction, Examples, Partitioning, Modification of Hierarchy, Optimization, Retiming, Technology mapping.	4
4.2	Formal Verification: Model checking, Equivalence checking, Fundamental techniques, Sequential circuits, Correctness of Synthesis steps, Design verification.	4
	Module 5: Geometric Layout and Geometric Verification	
5.1	Layout of CMOS circuits: layers in CMOS layout, latch-up speCIEl requirements for analog layout, substrate noise Devices in CMOS : resistors, capacitors, diodes, BJT; Data formats: LEF Data format, GDSII Data format	2
5.2	Standard cell Layout: standard cells, abstract view, floor planning, placement, routing	2
5.3	Geometric Verification: Introduction, Layer preprocessing, Design Rule check, Extract, Extraction of parasitic capacitors and resistors, ERC, LVS.	3

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E104B**

Course Name: EDA TOOLS

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Using the example of a multiplier evaluate the differences between algorithmic and RTL level descriptions for Integrated chips.
2. Evaluate the steps for logical synthesis? With the help of the below codes discuss the differences in the synthesized code.

```
...
c := a + b;
d := a - b;
IF(sub = '1')
THEN
   result <= d;
ELSE
   result <= c;
END IF;
```

```
...
IF(sub = '1')
THEN
   b := - b;
END IF;

result <= a + b;
```

Fig 1

3. Apply the SDF format for standardized digital models? Make a comparison with Explain Timing Back Annotation with a neat diagram?
4. How does optimization constraints such as time affect the delay and area of a chip? Give graphs to evaluate your argument.
5. Analyse synopsys design rule and optimization constraints related to area, delay and timing.

PART B

Answer any five questions. Each question carries 8 marks.

6. Giving a block diagram, analyse the structure of a Digital simulator? What are the logic values assoCIEted with the simulator? Briefly discuss the functional simulation of the following circuit:

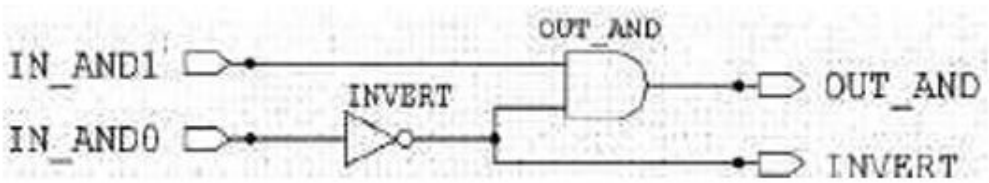


Fig 2

7. Evaluate the Model checking method of formal verification to prove the correctness of a circuit s=a+b+c+d for non negative binary numbers of length n bits? Use a 4 to 2 reduction circuit for the verification method?

8. Differentiate the concepts of fault collapsing and dominance with an example?

9. Evaluate the geometric layout methods giving the example of an Inverter circuit? Give a definition for LVS? What are the rules followed for DRC?

10. By giving a neat diagram evaluate the simultaneous controllability and observability by means of scan registers?

11. Discuss the construction of Standard cells for Digital library? How are the cells characterized?

12. Explain with neat diagram the Boundary scan standards to address the board level testing?

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E104C	DSP ALGORITHMS AND ARCHITECTURE	PROGRAM ELECTIVE I	3	0	0	3	3

Preamble: This course aims to familiarize the architecture of different DSP processors and its implementation in real time applications. The course also analyses the concepts of pipelining and dynamic scheduling in DSP algorithms.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Have good understanding of the architecture of different processors
CO 2	Analyse the architecture of Blackfin and TMS320C64x processors
CO 3	Apply the concepts of pipelining & Dynamic scheduling
CO 4	Design FIR and IIR filter using different methods
CO 5	Interface the DSP processor in real time applications

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1			3	4		
CO 2		2				
CO 3				4		
CO 4			2			
CO 5					5	

Assessment Pattern

Course name	DSP ALGORITHMS AND ARCHITECTURE		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar*	: 10 marks
Course based task/Micro Project//Data collection and interpretation/Case study	: 10 marks
Test paper 1 (Module 1 and Module 2)	: 10 marks
Test paper 2 (Module 3 and Module 4)	: 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answerquestions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of whichstudent shall answer any five. Each question can carry 8 marks. Total duration of theexamination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

INTRODUCTION TO COMPUTER ARCHITECTURE:
Introduction, Role of computer architecture in daily life. Von Neumann versus Harvard Architecture, CISC & RISC Architecture. Architectures of superscalar and VLIW processors. Pipelined Superscalar processors and Comparison of CISC, RISC & VLIW.

MODULE 2 (8 hours)

DETAILED ARCHITECTURE OF DIFFERENT PROCESSORS:
Introduction, CommerCIEl digital Signal-processing Devices - Architecture Details of Black Fin processor (Analog Devices), Core processor interfacing, memory access & different operations performed by ALU. Architecture, Data Addressing Modes, Memory Space of TMS320C64x Processors, Program Control & On-Chip peripherals, Interrupts of DSP processor TMS320C64x. Applications of the above processors.

MODULE 3 (8 hours)

CONCEPTS – PIPELINING & DYNAMIC SCHEDULING Basic pipeline:
Implementation details-pipeline hazards (based on MIPS 4000). Dynamic hardware prediction- Tomasulo's algorithm-Reducing data hazards and branch hazards. Multiple issuehardware-based speculation.

MODULE 4 (9 hours)

DIGITAL FILTER DESIGN & BILINEAR TRANSFORMATION:
Review of digital filter design: FIR & IIR filters – Difference equation and Transfer function Direct form I & II structures. Design example of FIR filter using window method. IIR filter design – Analog to digital transformation. Impulse Invariance and Bilinear transformation-Frequency warping. Example problems on IIR filter design.

MODULE 5 (7 hours)

DSP PROCESSORS INTERFACING IN REAL TIME APPLICATIONS:
Introduction, Synchronous Serial Interface, CODEC Interface Circuit, DSP hierarchical memory architecture, programming optimization guidelines, Real-life applications using DSP TMS320C family-MP3 voice recorder–player, Bio-telemetry Receiver, Speech Processing System.

Text Books

1. J. L. Hennesy, D.A. Patterson, "Computer Architecture A Quantitative Approach", 3/e, Elsevier India
2. Proakis, J.G. & Manolakis, D.G., "Digital Signal Processing: Principles, Algorithms & Applications", 3/e Prentice Hall of India, 1996.
3. Ifeachor, E.C. & Jervis, B.W., "Digital Signal Processing: A Practical Approach",2/e, Pearson Education Asia, 2002.
4. Nasser Kehtarnavaz, "Real Time Signal Processing Based on TMS320C6000", Elsevier, 2004.

COURSE CONTENTS AND LECTURE SCHEDULE

No	TOPIC	No. of Lecture/ Tutorial hours
	INTRODUCTION TO COMPUTER ARCHITECTURE	
1.1	Introduction, Role of computer architecture in daily life.	1
1.2	Von Neumann versus Harvard Architecture, CISC & RISC Architecture.	3
1.3	Architectures of superscalar and VLIW processors.	2
1.4	Pipelined Superscalar processors and Comparison of CISC, RISC & VLIW	2
	DETAILED ARCHITECTURE OF DIFFERENT PROCESSORS	
2.1	Introduction, CommerCIEl digital Signal-processing Devices	1
2.2	Architecture Details of Black Fin processor (Analog Devices), Core processor interfacing, memory access & different operations performed by ALU.	2
2.3	Architecture of DSP processor TMS320C64x. Data Addressing Modes of TMS320C64x. Memory Space of TMS320C64x Processors, Program Control	3
2.4	On-Chip peripherals of TMS320C64x Processor Interrupts of TMS320C64x Processor, Applications of this processor	2

	CONCEPTS – PIPELINING & DYNAMIC SCHEDULING	
3.1	Basic pipeline: implementation details-pipeline hazards (based on MIPS 4000)	2
3.2	Dynamic hardware prediction- Tomasulo's algorithm	3
3.3	Reducing data hazards and branch hazards	2
	Multiple issue- hardware-based speculation	1
	DIGITAL FILTER DESIGN & BILINEAR TRANSFORMATION	
4.1	Review of digital filter design: FIR & IIR filters – Difference equation and Transfer function Direct form I & II structures.	2
4.2	Design example of FIR filter using window method	2
4.3	IIR filter design – Analog to digital transformation. Impulse Invariance and Bilinear transformation Frequency warping	3
4.4	Example problems on IIR filter design	2
	DSP PROCESSORS INTERFACING IN REAL TIME APPLICATIONS	
5.1	Introduction, Synchronous Serial Interface, CODEC Interface Circuit	2
5.2	DSP hierarchical memory architecture, programming optimization guidelines	2
5.3	Real-life applications using DSP TMS320C familyMP3 voice recorder–player, Bio-telemetry Receiver, Speech Processing System.	3

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E104C**

Course Name: **DSP Algorithms and Architecture**

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. What is superscalar processor? Explain its design characteristics.
2. Briefly explain the interrupts of DSP processor TMS320C64x.
3. Explain briefly the technique of reducing data hazards.
4. Derive the frequency warping equation $\omega_a = \frac{2}{T}\tan\frac{\omega_d T}{2}$ $\omega_a = \frac{2}{T}\tan\frac{\omega_d T}{2}$.
5. Explain with the neat diagram the operation of pitch detector.

PART B

Answer any five questions. Each question carries 8 marks.

6. Explain briefly VLIW architecture, after drawing its schematic. Compare any 3 architecture characteristics of RISC, CISC and VLIW
7. Explain the architecture of BLACKFIN processor, with the help of a neat block diagram
8. Draw the block diagram of TMS320C64x architecture and briefly explain each block.
9. With the help of a block diagram explain branch optimized MIPS pipeline data path.
10. Illustrate Tomasulo's algorithm for dynamic scheduling, with the help of a neat block diagram.
11. Design a linear phase FIR low pass filter using rectangular window by taking 7 samples of window sequence

$$\omega_c = 0.4\pi\, rad/sample$$

and with a cut off frequency.

12. Explain the real time implementation of the processor TMS320C64X in an MP3 voice recorder–player, with neat schematics.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E104D	ADVANCED DIGITAL SIGNAL PROCESSING	PROGRAM ELECTIVE 1	3	0	0	3	3

Preamble: Through this course students can understand discrete/ and Fast Fourier transforms in depth for signal analysis. Students are equipped to design appropriate digital filters for signal processing applications. Students will know about Model parameter estimation techniques. They will get familiarized with the fundamentals of multirate digital signal processing.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Get a deep knowledge of designing various filters for signal processing
CO 2	Study the algorithms used for signal processing
CO 3	Develop the capacity to propose better filter designs and algorithms for various applications
CO 4	Understand the theory of multi rate digital signal processing
CO 5	Familiarize the applications of signal processing in different domains

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1			3	3	3	1
CO 2	1		3	3	2	
CO 3	2		3	3	3	2
CO 4	1		2	2	2	1

Assessment Pattern

Course name	ADVANCED DIGITAL SIGNAL PROCESSING		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Review on digital signal processing basics: Review of Frequency and time domain analysis -Discrete Fourier Transforms. Digital Filters-IIR Filters–Bilinear transformation, FIR filters– Windowing method, Finite wordlength effect Problems.

MODULE 2 (8 hours)

Linear and Adaptive Filter Design: Linear prediction & optimum linear filters, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction, Adaptive Filters , Minimum mean square criterion.

MODULE 3 (8 hours)

Power Spectrum Estimation: Parametric Methods for Power Spectrum Estimation: Relationship between the

auto correlation and the model parameters, Estimation methods for AR model parameters. Non parametric spectrum estimation, Periodogram- Bartlett's method-Minimum variance estimation.

MODULE 4 (9 hours)

Memory Test and Delay Test: Memory Faults, Fault Manifestations, Failure Mechanisms, March Test Notations, Fault Modeling, Reduced Functional Faults, Relation between Fault Models and Physical Defects, Delay Test Problem, Test Generation for Combinational Circuits, Transition Faults, Delay Test Methodologies.

MODULE 5 (7 hours)

DFT and BIST: Ad-Hoc DFT Methods, Scan Design Rules, Tests for Scan Circuits, Overheads of Scan Design, Partial-Scan Design, Variations of Scan, Random Logic BIST – BIST Process, BIST Implementations, Pseudo Random Pattern Generation using Standard LFSR, using Modular LFSR, BIST Response Compaction using LFSR, Multiple Input Signature Register.

Reference Books

1. J.G.Proakis and D.G.Manolakis"Digital signal processing: Principles, Algorithm and Applications", 4th Edition, Prentice Hall, 2007.
2. N. J. Fliege, "Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets", 1st Edition, John Wiley and Sons Ltd, 1999.
3. Bruce W. Suter, "Multirate and Wavelet Signal Processing",1st Edition, Academic Press, 1997.
4. M. H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley & SonsInc., 2002.
5. S.Haykin, "Adaptive Filter Theory", 4th Edition, Prentice Hall, 2001.
6. Fredric J Harris, Multirate Signal Processing for Communication Systems, 1st Edition, Pearson Education, 2007.

COURSE CONTENTS AND LECTURE SCHEDULE

(For 4 credit courses, the content can be for 45 hrs. and for 3 credit courses, the content can be for 36 hrs.)

No	Topic	No. of Lecture/ Tutorial hours
	Module 1 **Review on digital signal processing basics**	**8 hours**
1.1	Review of Frequency and time domain analysis -Discrete Fourier Transforms	2
1.2	Digital Filters-IIR Filters–Bilinear transformation	2
1.3	FIR filters– Windowing method	2
1.4	Finite wordlength effect Problems	2
	Module 2 **Linear and Adaptive Filter Design**	**8 hours**
2.1	Linear prediction & optimum linear filters	2
2.2	AR Lattice and ARMA Lattice-Ladder Filters	2
2.3	Wiener Filters for Filtering and Prediction	1
2.4	Adaptive Filters	2

2.5	Minimum mean square criterion	1
	Module 3 **Power Spectrum Estimation**	**8 hours**
3.1	Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters	1
3.2	Estimation methods for AR model parameters	2
3.3	Non parametric spectrum estimation, Periodogram	2
3.4	Bartlett's method	1
3.5	Minimum variance estimation	2
	Module 4 **Memory Test and Delay Test**	**9 hours**
4.1	Multi rate DSP - Decimators and Interpolators	2
4.2	Sampling rate conversion	1
4.3	Multistage decimator & interpolator	2
4.4	Poly phase filters	2
4.5	Digital filter banks- two channel quadrature mirror filter banks	1
4.6	M-channel QMF bank	1
	Module 5 **DFT and BIST**	**7 hours**
5.1	Application of DSP & Multi rate DSP	1
5.2	Application to Radar	1
5.3	Biomedical signal processing application	1
5.4	Application to image processing	1
5.5	Design of phase shifters	1
5.6	Use of DSP in speech processing	1
5.7	Multirate DSP Applications in sub-band coding	1

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E104D**

Course Name: ADVANCED DIGITAL SIGNAL PROCESSING

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. With neat diagrams, explain the performance specifications of IIR filters?
2. What are the practical limitations of the basic LMS algorithm?
3. Describe the computational requirements for Bartlett power spectrum estimate.
4. Discuss a method to decrease the sampling rate of a signal by an integer factor D.
5. Explain the application of DSP in speech processing.

PART B

Answer any five questions. Each question carries 8 marks.

6. An ideal high pass filter has a passband specified as, $\pi/4 \leq |\omega| \leq \pi$. Find the filter coefficients for the linear phase FIR filter with N = 11 (number of coefficients of the filter) using the Hanning window.
7. Explain the RLS adaptive algorithm.
8. What do you mean by periodogram? Explain the methods used for the computation of power density spectrum of random signals?
9. With the required expressions, illustrate how Reconstruction of the signal takes place in QMF Bank.

10. Explain the Wiener Filter based prediction algorithm.

11. Illustrate the use of Multirate digital signal processing in sub-band coding.

12. An ideal lowpass filter has a passband specified as, $-\frac{\pi}{2} \leq |H(e^{jw})| \leq \frac{\pi}{2}$. Find the filter coefficients, transfer function of realizable filter and magnitude of frequency response for the linear phase FIR filter with N = 11(number of coefficients of the filter)?

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E104E	ELECTRONIC PACKAGING	PROGRAM ELECTIVE 1	3	0	0	3	3

Preamble: Electronic packaging has emerged as a competent field in the world of semiconductor manufacturing. This course intends to provide a basic knowledge of the technologies and processes required for the packaging of electronic products. The focus of the course will be on the packaging techniques and reliability studies of electronic packages.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs. After the completion of the course the student will be able to

CO 1	Select appropriate materials and techniques for the fabrication of an electronics package as per given application
CO 2	Understand various packaging techniques used in IC industry
CO 3	Understand the various steps in IC Assembly, Wafer level packaging and PCB manufacturing
CO 4	Analyze thermal management issues in IC packaging
CO 5	Analyze the failure mechanism in an electronics package
CO 6	Design a cooling technique for thermal management

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3					
CO 2		2				
CO 3			1	2	1	1
CO 4	2			1		
CO 5		3	2		2	
CO 6						2

Assessment Pattern

Course name	ELECTRONIC PACKAGING		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (6 hours)

Microsystems Packaging- Need of packaging, challenges in IC packaging, Role of packaging in computer industry, telecommunication industry, automotive industry, medical electronics and consumer electronics

Packaging Materials – electrical, thermal, mechanical and chemical properties, Future trends.

Fundamentals of electrical package design -anatomy of systems packaging, signal distribution, power distribution, Electromagnetic interference

MODULE 2 (7 hours)

Single Chip Packaging- Functions, Types, Fundamentals, characteristics, materials

Multi-chip packaging- Multichip modules, functionality, advantages, multichip module technology comparisons, materials

RF packaging- Structure of RF systems, Fundamentals of RF packaging, Techniques for RF measurement, materials

MODULE 3 (9 hours)

IC Assembly- Need and Requirements of IC Assembly, wire bonding, Tape automated Bonding, Flip chip technology, materials

Wafer level packaging- Need and requirements for wafer level packaging, WLP technologies, Reliability aspects of WLP, Wafer-level Burn in and Test, Materials

Printed Circuit Board –Board Assembly, Surface Mount Technology, Through-Hole Technology, Assembly Issues, Design challenges, materials

MODULE 4 (10 hours)

Thermal Management – Need for thermal management, Fundamentals of thermal management, Thermal management of IC and PCB packages, Cooling Requirements, Electronic cooling methods

Sealing and Encapsulation: Encapsulation requirements, Encapsulation materials, Encapsulation processes, Hermetic Sealing, materials

MODULE 5 (8 hours)

Design for Reliability – microsystems failure and failure mechanisms, thermo mechanically induced failures, Electrically induced failures, chemically induced failures-Accelerated Testing

Electrical Testing- Need for Electrical testing, system level electrical testing, interconnection tests, active circuit testing

Reference Books

1. Rao R. Tummala: Fundamentals of Microsystem Packaging McGraw Hill
2. Richard K. Ulrich &William D. Brown Advanced Electronic Packaging - 2nd Edition: IEEE Press
3. Charles A Harper, Electronic Packaging and Interconnection Handbook, McGraw hill, Fourth Edition

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Basic concepts of systems packaging,	1
1.2	Role of packaging in computer industry, telecommunication industry, automotive industry, medical electronics and	1

	consumer electronics	
1.3	Electrical and Thermal properties of packaging materials	1
1.4	Mechanical and Chemical properties of packaging materials	1
1.5	Power distribution and signal distribution aspects in an electrical package	1
1.6	Electromagnetic interference issues	1
	Module 2	
2.1	Single Chip Packaging- Functions, Types, Fundamentals	1
2.2	Multichip packaging modules, functionality, advantages	1
2.3	Multichip module technologies -programmable, non-programmable	1
2.4	Non programmable MCM- MCM L, MCM C , MCM D	1
2.5	MCM C – LTCC and HTCC	1
2.6	MCM physical design cycle-partitioning, placement and routing	1
2.7	Fundamentals of RF packaging	1
	Module 3	
3.1	IC assembly fundamentals	1
3.2	Wire bonding	1
3.3	Tape automated Bonding	1
3.4	Flip chip technology	1
3.5	Need and requirements for wafer level packaging	1
3.6	Wafer level chip scale packaging	1
3.7	Surface Mount Technology-BGA/PLCC/QFP	1
3.8	Through-Hole Technology	1
3.9	Printed Circuit Board Assembly Issues	1
	Module 4	
4.1	Fundamentals and Need for thermal management	1
4.2	Thermal management of IC and PCB packages	1
4.3	Electronic cooling methods-Heat Pipes-Heat Sinks-Thermal vias	1
4.4	Design of heat sinks for packages	1
4.5	Design of Heat Pipes for cooling	1
4.6	Encapsulation process –Plastic, Non-Hermetic	1
4.7	Materials used for encapsulation/sealing	1
4.8	Glass sealing	1
4.9	Hermetic Sealing	1
4.10	Electron Beam sealing	1
	Module 5	
5.1	Thermo mechanically induced failures	1
5.2	Electrically induced failures	1
5.3	Chemically induced failures	1
5.4	System-level electrical testing	1
5.5	Active circuit testing	1
5.6	Interconnection tests	1
5.7	Reliability aspects of WLP, Wafer level Burn in and Test	1
5.8	Accelerated Degradation Modeling, Environmental Stress Screening	1

		Total	40

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E104E**

Course Name: Electronic Packaging

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. List the key elements to determine what kind of IC package would best suit the needs of the application?
2. Describe RF packaging requirements.
3. Differentiate axial and radial leads in through hole technology
4. Illustrate the working of thermal vias as a cooling technique for electronic systems
5. Explain chemically induced failures in an electronic system

PART B

Answer any five questions. Each question carries 8 marks.

6. Explain EMI issues in electronic packaging. Discuss any three methods to minimize EMI in electronic packages
7. Explain MCM physical design cycle
8. Explain 3 D packaging in detail
9. Illustrate how a suitable exit route be determined in a BGA layout
10. Suppose one need to package an application which should be sealed against atmosphere atmospheric, which sealing technique should be adopted. Illustrate the steps involved
11. Suggest a technique by which we can detect early failures in a batch of electronic devices
12. Suppose a sensor incorporating platinum is designed to monitor air quality. Since platinum is present, the sensor performance degrades in the presence of carbon monoxide. Devise an accelerated testing scheme so as to study the degradation caused to sensor by carbon monoxide.

SEMESTER I
PROGRAM ELECTIVE II

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E105A	ADVANCED DIGITAL SYSTEM DESIGN	PROGRAM ELECTIVE 2	3	0	0	3	3

Preamble:

●The student will learn analysis and synthesis of combinational and sequential circuits.
●Learn the principles of digital design and practices using data path components such as counters, shift registers, and adders etc.
●To introduce Register Transfer Level (RTL) design.
●The student will learn about optimizations and trade-offs in combinational logic, sequential logic, data path component and RTL design.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Create and analyze combinational and sequential circuits.
CO 2	Design circuits using data path components such as counters, shift registers, adders etc.
CO 3	Analyze Synchronizer Failure and Metastability
CO 4	Understand Register Transfer Level (RTL) design
CO 5	Understand optimizations and trade-offs in combinational logic, sequential logic, data path components and RTL design

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1		3	4	5	
CO 2	1		3	4	5	
CO 3	1		3	4	5	
CO 4	1		3		5	
CO 5	1		3	4	5	

Assessment Pattern

Course name	ADVANCED DIGITAL SYSTEM DESIGN		
Bloom's Category	**Continuous Internal Evaluation**		**End SemesterExamination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Combinational Logic Design Principles: Switching Algebra. Combinational-Circuit Analysis, Combinational- Circuit Synthesis. Programmed Minimization Methods, Timing Hazards, Sequential Logic Design Principles : Latches, flip flops, timing and glitches, Finite State Machines, Standard Controller Architecture for Implementing an FSM as a Sequential Circuit

MODULE 2 (8 hours)

Combinational Circuit Documentation Standards, Datapath Components: Registers, Adders Comparators, Multiplier—Array-Style, Subtractors and Signed Number, Arithmetic- Logic Units—ALUs, Shifters, Counters and Timers, Register Files

MODULE 3 (8 hours)

Synchronous Design Methodology- synchronous system structure, Impediments to Synchronous Design: clock skew, gating the clock synchronizer failure, asynchronous inputs, Synchronizer Failure and Metastability, Reliable synchronizer design, Analysis of metastable timing, better synchronizers

.MODULE 4 **(8 hours)**

Register-Transfer Level (RTL) Design: High-Level State Machine, RTL Design Process, Determining Clock Frequency, Behavioural-Level Design: C to Gates, Memory Components, Queues, FIFOs, Multiple Processors

MODULE 5 (8 hours)

Optimizations and Tradeoffs: Combinational Logic Optimizations and Tradeoffs, Sequential Logic Optimizations and Tradeoffs, Data path Component Tradeoffs, RTL Design Optimizations and Tradeoffs

Reference Books

1) Frank Vahid, "Digital Design with RTL Design, VHDL and Verilog", 2/e, Wiley, 2010
2) John F. Wakerly, "Digital Design Principles and Practices", 4/e, Prentice Hall, 2005.
3) William James Dally, R. Curtis Harting, "Digital Design: A Systems Approach", Cambridge University Press, 2012.
4) Randy H. Katz and Gaetano Borriello , "Contemporary Logic Design", 2/E, Prentice Hall India, 2009.
5) Harris & Harris, "Digital Design and Computer Architecture", 2/e, Morgan Kaufmann, 2012.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	**Combinational Logic Design Principles**	
1.1.1	Switching Algebra	0.5
1.2	Combinational-Circuit Analysis	0.5
1.3	Combinational- Circuit Synthesis	1
1.3.1	Programmed Minimization Methods	1
1.4	Timing Hazards	1
1.5	**Sequential Logic Design Principles**	
1.5.1	Latches, flip flops, timing and glitches	2
1.5.2	Finite State Machines	1
1.5.3	Standard Controller Architecture for Implementing an FSM as a Sequential Circuit	1
	Module 2	

2.1	**Combinational Circuit Documentation Standards**	
2.1.1	Combinational Circuit Documentation Standards	1
2.2	**Datapath Components:**	
2.2.1	Registers, Adders	1
2.2.2	Comparators, Multiplier—Array-Style	2
2.2.3	Subtractors and Signed Number, Arithmetic- Logic Units—ALUs	2
2.2.4	Shifters, Counters and Timers, Register Files	2
	Module 3	
3.1	**Synchronous Design Methodology**	
3.1.1	synchronous system structure	1
3.2	**Impediments to Synchronous Design:**	
3.2.1	clock skew	1
3.2.2	gating the clock synchronizer failure,	1
3.2.3	asynchronous inputs	1
3.3	**Synchronizer Failure and Metastability,**	
3.3.1	Synchronizer Failure, Reliable synchronizer design	2
3.3.2	Analysis of metastable timing, Better synchonizers	2
	Module 4	
4	**Register-Transfer Level (RTL) Design**:	
4.1	High-Level State Machine,	2
4.2	RTL Design Process	2
4.3	Determining Clock Frequency	1
4.4	Behavioural-Level Design: C to Gates	0.5
4.5	Memory Components, Queues- FIFOs	2
4.6	Multiple Processors	0.5
	Module 5	
5	Optimizations and Tradeoffs:	
5.1	Combinational Logic Optimizations and Tradeoffs	2
5.2	Sequential Logic Optimizations and Tradeoffs	2
5.3	Data path Component Tradeoffs	2
5.4	RTL Design Optimizations and Tradeoffs	2

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E105A**

Course Name: **ADVANCED DIGITAL SYSTEM DESIGN**

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Design a circuit, using four registers, that stores the four values present at an 8 bit input D during the previous four clock cycles. The circuit should have a single 8-bit output that can be configured using two inputs s1 and s0 to output any one of the four registers (hint: use an 8-bit 4 x 1 mux)
2. Design a 4-bit register with 2 control inputs s1 and s0, 4 data inputs I3, I2, I1 and I0 and 4 data outputsQ3, Q2, Q1 and Q0. When s1s0 = 00, the register maintains it's value. When s1s0 = 01, the register loads I3..I0. When s1s0 = 10, the register clears itself to 0000. When s1s0 = 11, the register reverses it's bits, so 1110 would become 0111, and 1010 would become 0101
3. Write notes on synchronous failure
4. Compose a 2048 x 8 ROM using only 256 x 8 ROMs
5. For the function F(a,b,c) = a'c + ac + a'b, determine all prime implicants and all essential prime implicants: using the tabular method.

PART B

Answer any five questions. Each question carries 8 marks.

6. Draw a state diagram for an FSM that has an input X and an output Y. Whenever X changes from 0 to 1, Y should become 1 for two clock cycles and then return to 0- even if X is still 1. (Assume that an implicit rising clock is ANDed with every FSM transition condition.)

7. Design a 4-bit up-counter that has two control inputs: cnt enables counting up, while clear synchronously resets the counter to all 0s:

(a) using parallel load register as a building block,
(b) using flip-flops and muxes

8. Write notes on clock skew

9. Use the RTL design process to create a 4-bit up-counter with input cnt (1 means count up), clear input clr, a terminal count output tc, and a 4-bit output Q indicating the present count.

10. Compare different types of memory. Describe various types of ROM?

11. Discuss various methods of state encoding with examples.

12. Explain the different optimizations and trade-offs implemented in RTL design with examples.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E105B	DIGITAL DESIGN PRINCIPLES AND APPLICATIONS	PROGRAM ELECTIVE II	3	0	0	3	3

Preamble:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

Course Outcomes: After the completion of the course the student will be able to

CO 1	Analyse and design synchronous and asynchronous sequential digital circuits.
CO 2	Design and use programming tools for implementing digital circuits of industry standards.
CO 3	Analyse different methods for fault identification and fault diagnosis in digital circuit.
CO 4	Examine the basic architecture and other features of different FPGAs.
CO 5	Understand modelling and verification with hardware description languages

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1			3	4		
CO 2				4	5	
CO 3			3	4	5	
CO 4				4	5	
CO 5			3	4		

Assessment Pattern

Course name	DIGITAL DESIGN PRINCIPLES AND APPLICATIONS		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	**CIE marks**	**ESE marks**	**ESE Duration**
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (5 hours)

SEQUENTIAL CIRCUIT DESIGN: Analysis of clocked synchronous sequential circuits and modelling - State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits ASM chart and realization using ASM.

MODULE 2 (10 hours)

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN: Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.

MODULE 3 (9 hours)

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS: Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Folded PLA‘s -Fault in PLA – Weinberger arrays – gate matrices – Test generation-DFT schemes – Built in self-test.

MODULE 4 (8 hours)

SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES: Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD.Capacitive parasitic - Capacitance and performance in CMOS – driving large capacitance – Resistive parasitic – Resistance and performance in CMOS. FPGA – Xilinx FPGA-Xilinx 4000 Programmable logic array designs – Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture – ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture.

MODULE 5 (8 hours)

SYSTEM DESIGN USING VERILOG: Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators for Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

Text Books

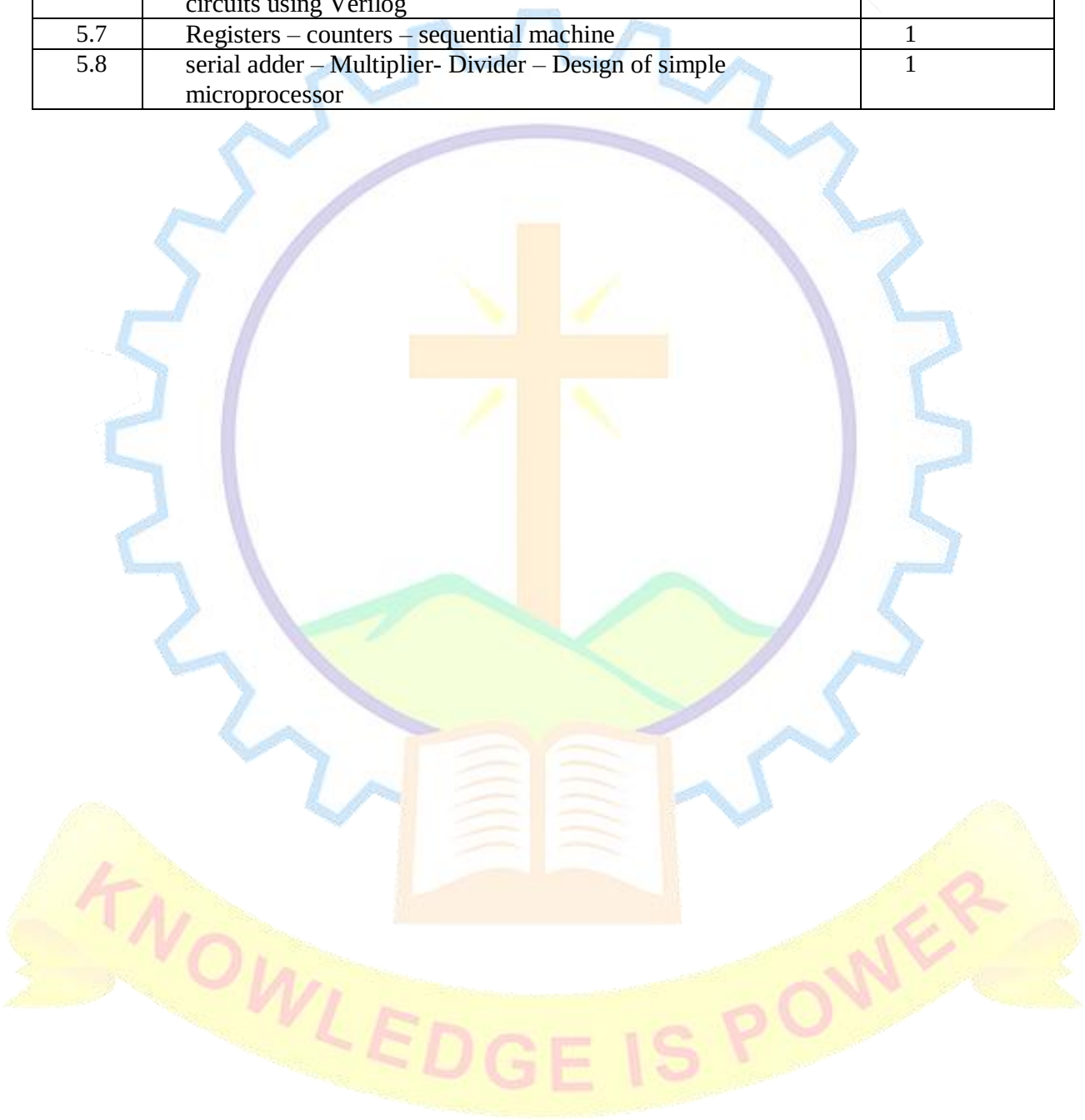
1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall,1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
5. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S
6. Parag K.Lala “Digital system Design using PLD” B S Publications,2003

7. Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, CreateSpace Independent Publishing Platform, Second Edition, 2015.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Analysis of clocked synchronous sequential circuits and modelling.	1
1.2	State diagram, state table, state table assignment and reduction-	2
1.3	Design of synchronous sequential circuits design of iterative circuits ASM chart and realization using ASM	2
	Module 2	
2.1	Analysis of asynchronous sequential circuit flow table reduction	2
2.2	races-state assignment-transition table and problems in transition table	2
2.3	Design of asynchronous sequential circuit	2
2.4	Static, dynamic and essential hazards	2
2.5	Data synchronizers – mixed operating mode asynchronous circuits	1
2.6	Designing vending machine controller	1
	Module 3	
3.1	Fault table method-path sensitization method	1
3.2	Boolean difference method-D algorithm	2
3.3	Tolerance techniques	1
3.4	The compact algorithm	1
3.5	Fault in PLA Folded PLA	2
3.6	Test generation-DFT schemes	1
3.7	Built in self-test	1
	Module 4	
4.1	Designing a synchronous sequential circuit using PLA/PAL –	1
4.2	Realization of finite state machine using PLD	1
4.3	Capacitive parasitic - Capacitance and performance in CMOS – driving large capacitance	2
4.4	Resistive parasitic – Resistance and performance in CMOS	1
	FPGA – Xilinx FPGA-Xilinx 4000 Programmable logic array designs	1
4.5	Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture –	1
4.6	ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture	1
	Module 5	
5.1	Hardware Modelling with Verilog HDL	1
5.2	Logic System, Data Types and Operators for Modelling in Verilog HDL	1

5.3	Behavioural Descriptions in Verilog HDL	1
5.4	HDL Based Synthesis – Synthesis of Finite State Machines	2
5.5	structural modelling – compilation and simulation of Verilog code	
5.6	Test bench - Realization of combinational and sequential circuits using Verilog	1
5.7	Registers – counters – sequential machine	1
5.8	serial adder – Multiplier- Divider – Design of simple microprocessor	1



Model Question Paper

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Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E105B**

Course Name: **DIGITAL DESIGN PRINCIPLES AND APPLICATION**

Max. Marks:60 Duration: 3 hours

PART A

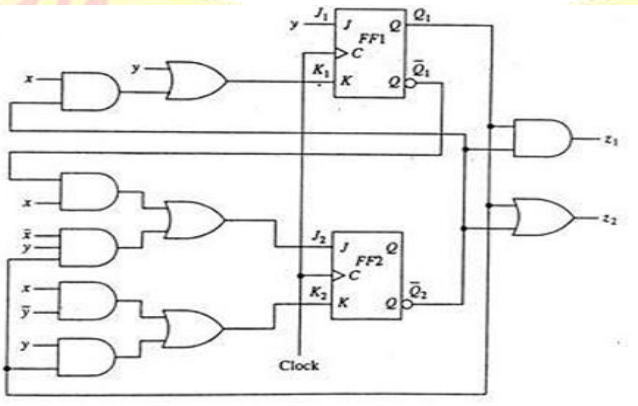
Answer all questions. Each question carries 4 marks.

1. Define Mealy and Moore model.
2. Write about static and dynamic hazards in combinational circuit.
3. Differentiate between truth table and D algorithm singular cover.
4. How does architecture of PAL differ from that of a PAL.
5. Write VHDL code for half adder.

PART B

Answer any five questions. Each question carries 8 marks.

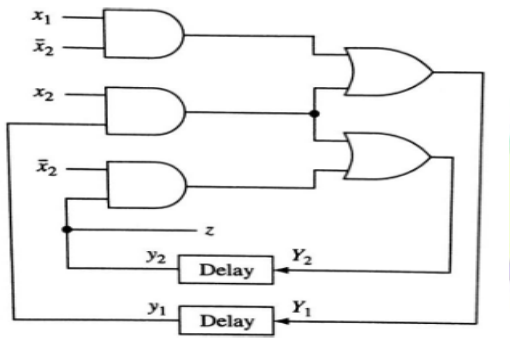
6. a. Design a synchronous sequential circuit for the count sequence 6- 4-3-7-1-6-4- 3-7-1...
b. For the clocked synchronous sequential circuit shown in figure construct transitiontable



7. **Design a coin-operated vending machine control unit which dispenses candy under the following conditions:**

- The machine accepts 5-cent coin and 10-cent coin only.
- It takes 10 cents for a piece of candy to be released from the machine.
- If 15 cents is deposited, the machine will not return the change, but it will credit the buyer with 5 cents and wait for the buyer to make a second purchase.

8. Write about races in asynchronous sequential circuit, and its elimination techniques with examples.
9. Analyze the asynchronous sequential circuit shown in figure by forming the excitation table/transition table, state table, flow table and flow diagram. The network operates in fundamental mode with restriction that only one input variable can change at a time.



10. Briefly write about the following terms with suitable examples
    a. path sensitization method
    b. Boolean difference method
11. Design a seven-segment display unit using suitable programmable logic devic
12. Design 4:1 multiplexer using behavioural modelling

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E105C	FUNCTIONAL VERIFICATION WITH SYSTEM VERILOG	PROGRAM ELECTIVE 2	3	0	0	3	3

Preamble: The purpose of this course is to provide a detailed explanation of Hardware verification language features and concepts used in the industry to verify the functional features of the digital system design, it speed up the verification process of the learner. Learner can construct a flexible and reliable verification environment from scratch. These environment components can be re-used across multiple projects. At the end of the course learner can build Bus Functional Models(BFMs)and evaluate the performance of the DUT based on Universal Verification Methodology (UVM)

Course Outcomes: After the completion of the course the student will be able to

CO 1	Understand the basics of Hardware verification and important features of Systemverilog for Hardware verification
CO 2	Able to design the Race free TestBench for Design Under Test(DUT)
CO 3	Analyze the performance evaluation of the design by using performance evaluation metrics
CO 4	Design of Verification IP(VIP) using Universal Verification Methodology(UVM)
CO 5	Design of Bus Functional Models(BFMs) for different applications

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1				4	5	
CO 2			3	4	5	
CO 3			3		5	
CO 4	1		3	4	5	
CO 5			3	4	5	5

Assessment Pattern

Course name	FUNCTIONAL VERIFICATION WITH SYSTEM VERILOG		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course-based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Basics of Verification: Verification Methodologies, Difference between verification & testing, Importance of hardware verification languages and methodologies.

Introduction to SystemVerilog: SystemVerilog data types, 4-state & 2-state types, typedefs, enum, struct data type.Packages, strings, static and dynamic type casting.

MODULE 2 (8 hours)

System Verilog operators and functions: loops in system Verilog, always blocks, tasks and functions case if and if-else statements, time scale. Structures, Arrays, Semaphores and Mailboxes: Structs and its assignments, packed and unpacked arrays, assoCIEtive arrays and methods, queues, semaphores and mailboxes.

Class and Extensions :System Verilog class basics, class declaration, class members and methods, class handles, 'super' and 'this' keywords, user defined constructors, class extension/ inheritance, new constructors, extending class methods, Virtual class, polymorphism using virtual methods.

MODULE 3 (8 hours)

Connecting the Testbench and Design: Test benches, Layered Organization of Test benches , Separating the Test bench and Design, Interface overview.
Program block: Fundamental test bench construction, program blocks, program block interaction with modules. Clocking: Clocking blocks, clocking skews, fork-join processes

MODULE 4 (8 hours)

Constrained Randomization: Random variables & built in-randomization methods, random sequence & examples, Randomization constraints, constraint distribution and set membership.

Coverage Metrics: Covergroups, coverpoints, coverpoint bins and labels, cross coverage.

MODULE 5 (8 hours)

UVM based Verification: UVM Environment components: Transaction, Sequence, Configuration Object, Driver, Sequencer, Monitor, Coverage collector Agent.
UVM Test Bench Architecture: Top, Test, Environment Agent & DUT Design of Bus Functional Models(BFMs)

Text Books

1. Chris Spear, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Springer-Verlag New York, Inc. Secaucus, NJ,USA, 2006
2. Mintz, Mike, Ekendahl, Robert, Hardware Verification with System Verilog, XXII, 314 p., Springer, ISBN: 978-0-387-71738-8 2007
3. Janick Bergeron Writing Testbenches using System Verilog, Springer
4. Stuart Sutherl, Simon Davidmann and Peter Flake (Author) System Verilog For Design: A Guide to Using SystemVerilog for Hardware Design and Modeling Kluwer Academic Publisher
5. http://www.asic-world.com/systemverilog/tutorial.html
6. http://www.vhdl.org/sv/SystemVerilog_3.1a.pdf
7. http://www.systemverilog.in

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Verification process flow diagram	1
1.2	Different verification methods	1
1.3	Difference between verification & testing	1
1.4	Importance of hardware verification languages	1
1.5	SystemVerilog supporting data types	1
1.6	Difference between 4-state & 2-state data types	1
1.7	Typedefs, enum, struct data type	1
1.8	Static and Dynamic data type casting.	1
	Module 2	
2.1	Types of loops in system Verilog,always blocks	2
2.2	Tasks and functions case if and if-else statements	1

2.3	Structures, Arrays, Semaphores and Mailboxes	1
2.4	Packed and unpacked arrays, assoCIEtive arrays	1
2.5	SystemVerilog class basics	
2.6	Class declaration,class members and methods	1
2.7	Class extension/inheritance, new constructors, extending class methods	1
2.8	Class declaration,class members and methods	1
	Module 3	
3.1	Layered Organization of Test benches	2
3.2	Separating the Testbench and Design,	1
3.3	Interface overview,modport	1
3.4	Program blocks	2
3.5	Clocking blocks, Clocking skews,	1
3.6	Fork-join processes	1
3.7	**Module 4**	
4.1	Constrained Randomization,weighted distrubution	2
4.2	Random variables & built in-randomization methods	1
4.4	Random sequence & examples	1
4.5	Randomization constraints, constraint distribution	1
4.6	Set membership	1
4.7	Covergroups, Coverpoints, coverpoint & bins	2
4.8	Module 5	
5.1	UVM based verification overview, Transaction,Sequence	2
5.2	Configuration Object,Driver	1
5.3	Sequencer,Monitor& Agent	1
5.4	Top &Test	1
5.5	Environment Agent & DUT	1
5.6	Design of Bus Functional Models(BFMs)	2

Model Question Paper

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Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E105C**

Course Name: **Functional Verification with SystemVerilog**

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Differentiate between **Verification and Validation** in SystemVerilog?
2. Differentiate between **Function and Task** in SystemVerilog? Explain with an example?
3. Justify how **Program block** is used to avoid **Race condition** in design of Test bench?
4. Explain the importance of weighted distribution in SystemVerilog? Explian with an example?
5. Explain Synchronization mechanism between Sequencer and Driver in UVM methodology?

PART B

Answer any five questions. Each question carries 8 marks.

6. a. Explain the verification flow of the Digital System Design?
7. a. Explain Procedural Assignment statements in SystemVerilog? Predict the simulator output of the below given program?

```
module block();
integer a,b,c;
initial begin
$monitor ("[%0t] a=%0d b =%0d c= %0d ", $time, a, b, c);
a=10;b=5;c=15;
#1 a=b+c;
#2 b=a+5;
#3 c=a-b;
```

EC5

```
end
endmodule
```

8. a. Design a Module and Test bench for 4:1 Multiplexer in SystemVerilog?

9. Explain how the **fork and Join** process works in SystemVerilog? Predict the simulator output of the below given program?

```
program main;
initial begin
$display(" First fork time = %d",$time );
 fork
begin #10;
$display("time1 = %d",$time);
end
begin
 #(5);
$display("time2 = %d",$time);
 #(2);
$display("time3 = %d",$time);
end
join
$display(" time = %d Outside the main fork ",$time );
end
endprogram
```

10. a . What are the performance evaluation metrics in SystemVerilog? Explian different types of constructs used for functional coverage implementation in systemverilog?

11. a. Design of SPI Master slave controller Verification IP (VIP) using UVM methodology in SystemVerilog ?

12. a. Design of Bus Functional Model(BFM) for Advanced Peripheral Bus (APB) protocol ?

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E105D	ASIC DESIGN	PROGRAM ELECTIVE 2	3	0	0	3	3

Preamble: The purpose of this course is to provide fundamentals in ASIC Design, Architecture and programmability. The Course describes the learning level of ASICs from the level of cell design, device simulation and synthesis. The concept of Logic design helps to under the subject in micro level. .

Course Outcomes: After the completion of the course the student will be able to

CO 1	Study the fundamentals of the ASIC. **(Cognitive Knowledge Level: Analyse)**
CO 2	Apply CMOS Designs based on rules and different logic cell element designs **(Cognitive Knowledge Level: Apply)**
CO 3	Evaluate the cell designs and architectures. **(Cognitive Knowledge Level: Evaluate)**
CO 4	Apply the programmable ASICs with solutions **(Cognitive Knowledge Level: Apply)**
CO 5	Evaluate the devices and synthesis followed. **(Cognitive Knowledge Level: Evaluate)**

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1		3	2		
CO 2	1		3	4		
CO 3	1		3	4		
CO 4	1		3	4		
CO 5			3	4	5	

Assessment Pattern

Course name	ASIC DESIGN		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (ASIC Fundamentals)

Introduction to ASICs-Types of ASICs: Full Custom ASICs, , Standard Cell based ASICs, Gate Array based ASICs, Channeled Gate Array, Channelless Gate Array, Structured Gate Array, Programmable Logic Devices, Field Programmable Gate Arrays. Design Flow, ASIC Cell Libraries.

MODULE 2 (CMOS Designs)

CMOS Transistors-CMOS Process, CMOS Design Rules, Combinational Logic Cells, Sequential logic Cells, Latch, Flip-flops, Clocked inverter. Data path logic Cells: Data path elements, Adders, Multipliers, I/O Cells, Cell Compilers.

MODULE 3 (Cell Designs and Architecture)

Transistors as Resistors-Transistors parasitic capacitance: Junction capacitance, Overlap capacitance, Gate

Capacitance, Slew Rate, Logical Effort: Predicting Delay, Logical Area and logical efficiency, Logical path, Multistage cells, Optimum delay, Optimum number of stages, Library Cell Design, Library Architecture, Gate Array Design, Standard Cell Design, Data Path Cell design.

MODULE 4 **(Programmability)**

Programmable ASICs- Antifuse, Static Ram, EPROM and EEPROM Technology, Practical issues, Specifications, Programmable ASIC logic cells: Actel ACT , Xilinx LCA, Altera Flex, Altera Max, Programmable ASIC I/O cells: DC output, AC Output, DC Input, AC Input, Clock Input, Power Input, Xilinx I/O block.

MODULE 5 (Devices and Synthesis**)**
Programmable ASIC Interconnect-Actel ACT, Xilnx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera Flex, VHDL, Verilog HDL, Logic Synthesis.

Text Books

1. "Application-Specific Integrated Circuits", Michael John Sebastian Smith June 1997.
2. "Application-Specific Integrated Circuits", Michael John Sebastian Smith, January 2002
3. Application Specific Integrated Circuit (ASIC) Technology", Norman G. Einspruch and Jeffrey L. Hilbert Published 1991
4. "High Performance ASIC Design", Razak Hossain, 2009

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1 **ASIC Fundamentals**	**8 hours.**
1.1	Introduction to ASICs-Types of ASICs: Full Custom ASICs,	1
1.2	Standard Cell based ASICs, Gate Array based ASICs,	1
1.3	Channelled Gate Array	1
1.4	Channelless Gate Array	1
1.5	Structured Gate Array	1
1.6	Programmable Logic Devices	1
1.7	Field Programmable Gate Arrays	1
1.8	Design Flow, ASIC Cell Libraries	1
	Module 2 **CMOS Designs**	**8 hours**
2.1	CMOS Transistors-CMOS Process,	1
2.2	CMOS Design Rules	1
2.3	Combinational Logic Cells	1
2.4	Sequential logic Cells, Latch	1
2.5	Flip-flops, Clocked inverter.	1
2.6	Data path logic Cells: Data path elements,	1
2.7	Adders, Multipliers	1
2.8	I/O Cells, Cell Compilers	1

	Module 3 Cell Designs and Architecture-	**8 hours**
3.1	Transistors as Resistors	1
3.2	Transistors parasitic capacitance: Junction capacitance,	1
3.3	Overlap capacitance, Gate Capacitance	1
3.4	Slew Rate,	1
3.5	Logical Effort: Predicting Delay, Logical Area and logical efficiency	1
3.6	Logical path, Multistage cells,	1
3.7	Optimum delay, Optimum number of stages, Library Cell Design	1
3.8	Library Architecture, Gate Array Design, Standard Cell Design, Data Path Cell design	1
	Module 4 **Programmability**	**8 hours**
4.1	Programmable ASICs- Antifuse,	1
4.2	Static Ram, EPROM and EEPROM Technology	1
4.3	Practical issues, Specifications, Programmable ASIC logic cells: Actel ACT,	1
4.4	Xilinx LCA, Altera Flex, Altera Max,	1
4.5	Programmable ASIC I/O cells: DC output,	1
4.6	AC Output, DC Input, AC Input, Clock Input	1
4.7	Power Input	
4.8	Xilinx I/O block	1
	Module 5 **Devices and Synthesis**	**8 hours**
5.1	Programmable ASIC Interconnect	1
5.2	Actel ACT, Xilnx LCA	1
5.3	Xilinx EPLD	1
5.4	Altera Max 5000 and 7000	1
	Altera Max 9000	1
	Altera Flex, VHDL	1
	Verilog HDL	1
	Logic Synthesis.	1

Model Question Paper

QP CODE: **Pages: 1**

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E105D**

Course Name: **ASIC Design**

Max. Marks:60 **Duration: 2.5 Hours**

PART A

Answer all questions. Each question carries 4 marks.

1. What are the types of ASICs?
2. Evaluate the channelled Gate Array and Channelless Array.
3. Sketch the CMOS and mention the rules.
4. What is the role adders and multipliers.
5. Give a detail account on the Library architecture used in the design.

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 8 marks.

6. Evaluate the architecture advantages of Xilinx LCA.
7. Evaluate the architecture in Altera Flex, Altera Max.
8. Find the AC Output, DC Input, AC Input, Clock Input with respect to the programmability of ASIC.
9. Explain the most Actel ACT, Xilnx LCA and analyse the features.
10. Analyse the usage of Altera Max 5000 and 7000 with examples.
11. Write a VHDL programme to control the digital input output system
12. Why Xilinix EPLD is having more superiority than other hardware's in terms of effciiency. Give the facts?

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E105E	EMBEDDED OPERATING SYSTEM	PROGRAM ELECTIVE II	3	0	0	3	3

Preamble: The purpose of this course is to provide a complete awareness of Embedded Operating Systems and Embedded Software Development. As an outcome of the course the students will be ready for OS porting, Embedded baremtal application development, Linux device driver development and RTOS porting.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Student will be enabled to write, compile and run baremtal application programs for embedded systems. **(Cognitive Knowledge Level: Apply)**
CO 2	Student will get knowledge on Operating systems internals like scheduling, memory management etc. **(Cognitive Knowledge Level: Analyse)**
CO 3	Introduction to an RTOS named FreeRTOS and familarization on developement of real world application on FreeRTOS **(Cognitive Knowledge Level: Apply)**
CO 4	Student will acquire knowledge on Linux internals, kernel modules, libraries, root file system etc. **(Cognitive Knowledge Level: Analyse)**
CO 5	Analyze the failure mechanism in an electronics package
CO 6	Student will be able to develop and run basic Linux device drivers **(Cognitive Knowledge Level: Apply)**

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1			3	4		
CO 2	0	2				
CO 3				4		
CO 4			3			
CO 5					5	

Assessment Pattern

Course name	EMBEDDED OPERATING SYSTEM		
Bloom's Category	**Continuous Internal Evaluation**		**End SemesterExamination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours): Embedded Software Development

Host and Target Machines, Toolchain for Embedded Software, Native versus cross compilers, Using a standard library, C extensions for Embedded Systems, Getting Embedded Software into the target system, Debugging Techniques, Testing on your host machine, Instruction Set Simulators, Baremetal programming, IDEs

MODULE 2 (8 hours): Operating Systems

What are Operating Systems, Operating System Internals, Multitasking Operating Systems, Scheduling, Scheduler Algorithms, Memory Management, Interrupts and its significance in real time processing, saving and restoring context, disabling interrupts, characteristics of shared data, atomic and critical sections, interrupt latency. Software Architectures: Round Robin, Round Robin with interrupts, Function Queue scheduling Architecture, Architecture selection.

MODULE 3 (8 hours): Real Time Operating Systems

Introduction to RTOS, Task and task states, Task and data, Semaphore and shared data. RTOS Architecture, Hard real time and Soft real time, Examples of CommerCIEl RTOS RTOS Services: Message Queues, Mail

boxes and pipes, Timer functions, events, Memory Management. Basic Design using an RTOS: Principle, Hard real time scheduling considerations, saving memory space, saving power, Real time application development using FreeRTOS.

MODULE 4 (8 hours): Linux

Linux Kernel, Linux internals, Kernel Considerations- selection, configuration , Compiling and Installing the Kernel Root File System structure, Libraries, Kernel Modules, Kernel Images, Device Files, Main System Applications, Custom Applications, System Initialization, Porting Kernel. Busy box, Root Filesystem Setup: Filesystem Types for Embedded Devices, Writing a Filesystem Image to Flash using an NFS-Mounted Root Filesystem, Placing a Disk Filesystem on a RAM Disk , Rootfs and Initramfs, Choosing a Filesystem's Type and Layout.

MODULE 5 (8 hours): Linux Device Drivers and Bootloaders

Introduction, Building and running modules, Character Drivers, Block device drivers, Net device drivers, Allocating memory. USB Drivers, Device Model, Memory mapping and DMA, Block Drivers, TTY Drivers. Setting Up the Bootloader: Embedded Bootloaders, Server Setup for Network Boot, Using the U-Boot Bootloader.

Text Books

1. Steve Heath, Embedded System Design, 2nd edition, Newnes.
2. David Simon Embedded Software Primer, Addison- Wesley, 1999.
3. Dr.K V K K Prasad, Embedded / Real time systems: Concepts, Design and Programming, Dream Tech press, New Delhi.
4. Frank Vahid,Tony D. Givargis, Embedded System Design- A Unified Hardware/ Software Introduction, John Wiley and Sons, Inc 2002.
5. D Jonathan W. Valvano,Embedded Microcomputer systems, Brooks / Cole, Thompson Learning. New Jersey.
6. Arnold S Burger, Embedded Systems Design - Introduction to Processes, Tools, Techniques", CMP books
7. Daniele Lacamera, Embedded Systems Architecture, O'Reilly
8. Max Back, freeRTOS: A practical approach with Arduino
9. Daniel P. Bovet & Marco Cesati, Understanding the Linux Kernel, O'Reilly
10. Jonathan Corbet, Alessandro Rubini, Greg Kroah-Hartman, Linux Device Drivers

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1: Embedded Software Development	
1.1	Host and Target Machines, Toolchain for Embedded Software	1
1.2	Native versus cross compilers, Using a standard library	1
1.3	C extensions for Embedded Systems	1
1.4	Getting Embedded Software into the target system	1
1.5	Debugging Techniques	1

1.6	Testing on your host machine, Instruction Set Simulators	1
1.7	Baremetal programming	1
1.8	IDEs	1
	Module 2: Operating Systems	
2.1	What are Operating Systems, Operating System Internals	1
2.2	Multitasking Operating Systems, Scheduling	1
2.3	Scheduler Algorithms, Memory Management	1
2.4	Interrupts and its significance in real time processing	1
2.5	saving and restoring context, disabling interrupts,characteristics of shared data	1
2.6	atomic and critical sections, interrupt latency	1
2.7	Software Architectures: Round Robin, Round Robin with interrupts	1
2.8	Function Queue scheduling Architecture, Architecture selection	1
	Module 3: Real Time Operating Systems	
3.1	Introduction to RTOS, Task and task states	1
3.2	Task and data, Semaphore and shared data	1
3.3	RTOS Architecture, Hard real time and Soft real time, Examples of CommerCIEl RTOS	1
3.4	RTOS Services: Message Queues, Mail boxes and pipes	1
3.5	Timer functions, events, Memory Management	1
3.6	Basic Design using an RTOS: Principle, Hard real time scheduling considerations, saving memory space, saving power,	1
3.7	Real time application development using FreeRTOS	1
3.8	Real time application development using FreeRTOS	1
	Module 4: Linux	
4.1	Linux Kernel, Linux internals	1
4.2	Kernel Considerations- selection, configuration	1
4.3	Compiling and Installing the Kernel Root File System structure	1
4.4	Libraries, Kernel Modules, Kernel Images, Device Files	1
4.5	Main System Applications, Custom Applications, System Initialization, Porting Kernel.	1
4.6	Busy box, Root Filesystem Setup: Filesystem Types for Embedded Devices	1
4.7	Writing a Filesystem Image to Flash using an NFS-Mounted Root Filesystem	1
4.8	Placing a Disk Filesystem on a RAM Disk, Rootfs and Initramfs, Choosing a Filesystem's Type and Layout	1
	Module 5: Linux Device Drivers and Bootloaders	
5.1	Introduction, Building and running modules	1
5.2	Character Drivers	1
5.3	Block device drivers	1
5.4	Net device drivers, Allocating memory	1
5.5	USB Drivers, Device Model, Memory mapping and DMA	1
5.6	Block Drivers, TTY Drivers	1
5.7	Setting Up the Bootloader: Embedded Bootloaders, Server Setup for Network Boot	1

5.8	Using the U-Boot Bootloader	1
	Total	40

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E105E**

Course Name: Embedded Operating Systems

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Define the terms host and target machines, native and cross compilers ?
2. Explain shared data, atomic and critical sections
3. What is the difference between hard real time and soft real time systems?
4. Explain the terms Kernel root file system, libraries, kernel modules and device files
5. Explain different types of Linux device drivers

PART B

Answer any five questions. Each question carries 8 marks.

6. Develop and compile a program in assembly and C language for ARM/ RISC-V architecture
7. Develop and compile a program in C language for ARM/ RISC-V architecture and debug the program on Instruction Set Simulator
8. Explain advantages and disadvantages of different Software Architectures like Round Robin, Function Que scheduling etc.
9. Explain a scenario on critical sections and provide its solution
10. Write a C program for Free RTOS demonstrating a real world application for RTOS

11. Create a rootfs structure for Linux and build the same for ARM /RISC-V
12. Write character and block device drivers, build for ARM/ RISC-V and test on an Instruction set simulator like QEMU

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1R106	Research Methodology & IPR	Theory	2	0	0	2	2

Preamble: This course introduces the strategies and methods related to scientific research. The students are also trained in the oral presentation with visual aids and writing technical thesis/reports/research papers. The salient aspects of publication and patenting along with the cruCIEl role of ethics in research is discussed.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Approach research projects with enthusiasm and creativity.
CO 2	Conduct literature survey and define research problem
CO 3	Adopt suitable methodologies for solution of the problem
CO 4	Deliver well-structured technical presentations and write technical reports
CO 5	Publish/Patent research outcome

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1						
CO 2						
CO 3						
CO 4						
CO 5						

Assessment Pattern

Course name	Research Methodology & IPR		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	2.5 Hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer reviewed (minimum 10 publications shall be referred)	Original publications in the relevant discipline : 10 marks
Course based task/Seminar/Quiz	: 10 marks
Test paper 1 (Module 1 and Module 2)	: 10 marks
Test paper 2 (Module 3 and Module 4)	: 10 marks

End Semester Examination Pattern: The end semester examination should be conducted by the college. The time duration will be for 3 Hrs and will contain 7 questions, with minimum one question from each module of which student should answer any five. Each question can carry 12 marks.

Reference Books

1. E. M. Phillips and D. S. Pugh, "How to get a PhD - a handbook for PhD students and their supervisors", Viva books Pvt Ltd.
2. G. L. Squires, "Practical physics", Cambridge University Press
3. Antony Wilson, Jane Gregory, Steve Miller, Shirley Earl, Handbook of Science Communication, Overseas Press India Pvt Ltd, New Delhi, 1st edition 2005
4. C. R. Kothari, Research Methodology, New Age International, 2004
5. Panneerselvam, Research Methodology, Prentice Hall of India, New Delhi, 2012.
6. Leedy P. D., Practical Research: Planning and Design, McMillan Publishing Co.
7. Day R. A., How to Write and Publish a Scientific Paper, Cambridge University Press, 1989.
8. William Strunk Jr., Elements of Style, Fingerprint Publishing, 2020
9. Peter Medawar, 'Advice to Young Scientist', Alfred P. Sloan Foundation Series, 1979.
10. E. O. Wilson, Letters to a Young Scientist, Liveright, 2014.
11. R. Hamming, You and Your Research, 1986 Talk at Bell Labs.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1: **Introduction**	
1.1	Meaning and significance of research, Skills, habits and attitudes for research, Types of research,	1
1.2	Characteristics of good research, Research process	1
1.3	Motivation for research: Motivational talks on research: "You and Your Research"- Richard Hamming	1
1.4	Thinking skills: Levels and styles of thinking, common-sense and scientific thinking, examples, logical thinking, division into sub-problems, verbalization, awareness of scale.	1
1.5	Creativity: Some definitions, illustrations from day to day life, intelligence versus creativity, creative process, requirements for creativity	1

	Module 2: **Literature survey Problem definition**	
2.1	Information gathering – reading, searching and documentation; types of literature. Journal index and impact factor	1
2.2	Integration of research literature and identification of research gaps	1
2.3	Attributes and sources of research problems; problem formulation, Research question, multiple approaches to a problem	1
2.4	Problem-solving strategies – reformulation or rephrasing, techniques of representation, Importance of graphical representation; examples	1
2.5	Analytical and analogical reasoning, examples; Creative problem solving using Triz, Prescriptions for developing creativity and problem solving	1
	Module 3: **Experimental and modelling skills**	
3.1	Scientific method; role of hypothesis in experiment; units and dimensions; dependent and independent variables; control in experiment	1
3.2	Precision and accuracy; need for precision; definition, detection, estimation and reduction of random errors; statistical treatment of data; definition, detection and elimination of systematic errors;	1
3.3	Design of experiments; experimental logic; documentation	1
3.4	Types of models; stages in modelling; curve fitting; the role of approximations; problem representation; logical reasoning; mathematical skills;	1
3.5	Continuum/meso/micro scale approaches for numerical simulation	1
	Module 4: **Effective communication - oral and written**	
4.1	Examples illustrating the importance of effective communication; stages and dimensions of a communication process.	1
4.2	Oral communication –verbal and non-verbal, casual, formal and informal communication; interactive communication; listening; form, content and delivery; various contexts for speaking- conference, seminar etc.	1
4.3	Guidelines for preparation of good presentation slides	1
4.4	Written communication - form, content and language; layout, typography and illustrations; nomenclature, reference and citation styles, contexts for writing – paper, thesis, reports etc. Tools for document preparation-LaTeX.	1
4.5	Common errors in typing and documentation	1
	Module 5: **Publication and Patents**	
5.1	Relative importance of various forms of publication; Choice of journal and reviewing process, Stages in the realization of a paper .	1
5.2	Research metrics-Journal level, Article level and Author level, Plagiarism and research ethics	1
5.3	Introduction to IPR, Concepts of IPR, Types of IPR	1
5.4	Common rules of IPR practices, Types and Features of IPR Agreement, Trademark	1
5.5	Patents- Concept, Objectives and benefits, features, Patent process – steps and procedures	1

Model Question Paper

QP CODE: Pages: X

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: M24EC1R106

Course Name: Research Methodology & IPR

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 5 marks

1. What are the characteristics of good research? Explain various types of research.
2. Explain the process of Literature review.
3. What is Design of Experiments (DOE)? Describe the need for DOE.
4. Describe the guidelines for the preparation of good presentation slides.
5. Briefly explain the choice of journal and reviewing process.
6. Explain the different types of IPR. Specify the objectives and benefits of patents.

Part B

7	Read the given article and write a report that addresses the following issues (The article given can be specific to the discipline concerned)	**Marks**
a	What is the main research problem addressed?	**4**
b	Identify the type of research	**4**
c	Discuss the short comings in literature review if any?	**4**
d	Discuss the significance of the study	**6**
e	Discuss appropriateness of the methodology used for the study	**6**
f	Summarize the important results and contributions by the authors	**6**

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1L107	HDL Lab	Laboratory	0	0	3	2	2

Preamble: The purpose of this course is to impart practical skills in developing a synthesizable digital sub system using Verilog HDL.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Study of HDL and various VLSI design tools. (Cognitive Knowledge Level: Analyse)
CO 2	Analyse a problem statement and design a solution based on the available tools and find results. (Cognitive Knowledge Level: Analyse)
CO 3	Design and synthesis HDL codes for combinational circuits. (Cognitive Knowledge Level: Evaluate)
CO4	Design and synthesis HDL codes for sequential circuits. (Cognitive Knowledge Level: Evaluate)
CO 5	Identify a practical problem and develop a solution, test and simulate using the available VLSI platform. (Cognitive Knowledge Level: Create)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1			2	2	1	1
CO 2	2		2	2	3	1
CO 3			2		1	1
CO 4			2		1	1
CO 5	2	3	2	2	3	2

Mark distribution

Total Marks	CIE Marks
100	100

Continuous Internal Evaluation Pattern:

Lab work and Viva-voce	: 60 marks
Final assessment Test and Viva voce	: 40 marks

The laboratory courses will be having only Continuous Internal Evaluation and carries 100 marks. Final assessment shall be done by two examiners; one examiner will be a senior faculty from the same department.

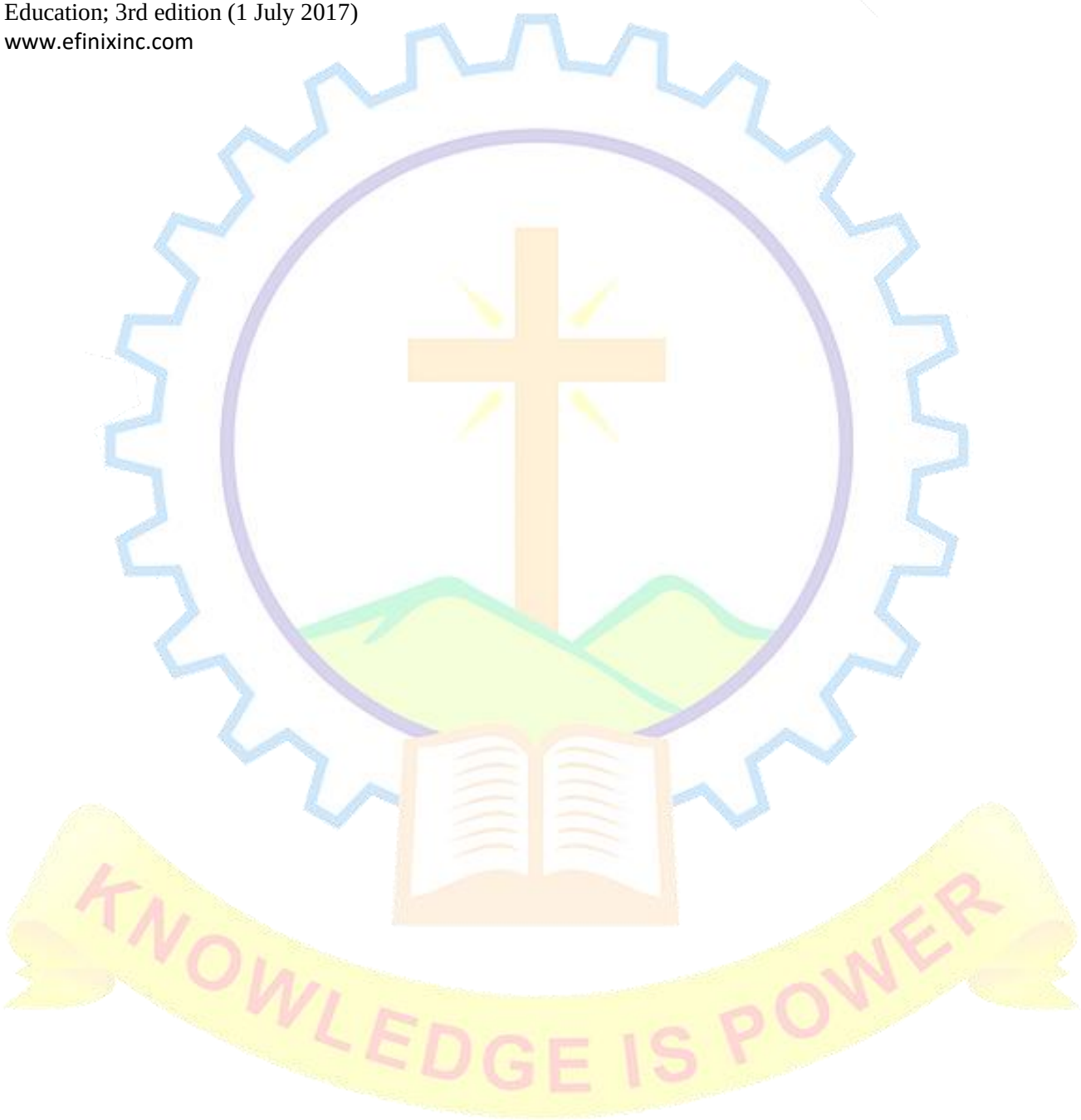
SYLLABUS

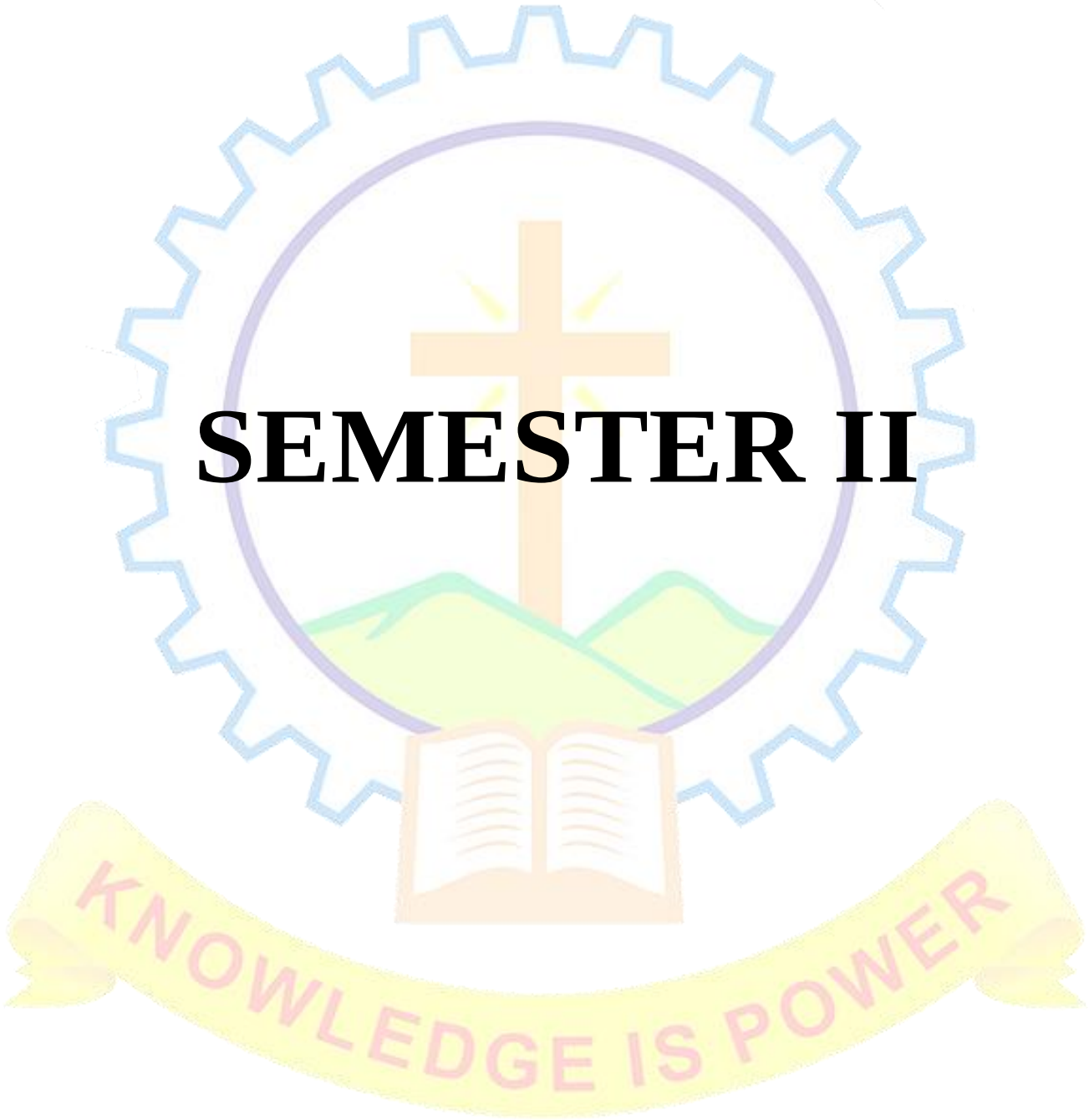
LIST OF EXPERIMENTS

1	Write HDL codes to find the highest number among three 4-bit numbers and demonstrate it using software simulation.
2	Write HDL codes to design 8-bit adder using instantiation and demonstrate it using software simulation.
3	Write HDL codes to realize multiplexers, encoders and decoders using software simulation.
4	Write HDL codes to design different types of shift registers and demonstrate it using software simulation.
5	Write HDL codes to design different types of binary counters and demonstrate it using software simulation.
6	Write HDL codes to design an 8-bit ALU using software simulation.
7	Write HDL codes to design a MAC using software simulation.
8	Write HDL codes to design register file using D flipflop and demonstrate it using software simulation.
9	Write HDL codes to design a controller for 4*4 LED matrix and demonstrate it using software simulation and hardware implementation.
10	Write HDL codes to design an 8-bit RAM using software simulation.
11	Write HDL codes to design and implement a Moore based rising edge detector and demonstrate it using software simulation.
12	Write HDL codes to design and implement a UART transmitter and demonstrate it using software simulation and hardware implementation.
13	Write HDL codes to design and implement a PWM module and demonstrate it using software simulation and hardware implementation.
14	Write HDL codes to design and implement a VGA controller and display lines, rectangles and circles and demonstrate it using software simulation and hardware implementation.

Reference books

1. Pong P. Chu, "FPGA Prototyping by Verilog Examples", John Wiley & Sons, 2008
2. J.Bhaskar, “VHDL Primer”, Pearson Education India; 3rd edition (1 January 2015)
3. J.Bhaskar, ”A VHDL Synthesis Primer”, Pearson Education, Second Edition
4. Charles H. Roth, Jr., Lizy K. John, ”Digital Systems Design Using VHDL”, 3rd Edition, Cengage Learning
5. Stephen Brown , Zvonko Vranesic, Fundamentals of Digital Logic with VHDL Design”, McGraw Hill Education; 3rd edition (1 July 2017)
6. www.efinixinc.com





SEMESTER II

Discipline: ELECTRONICS AND COMMUNICATION

Stream: VLSI AND EMBEDDED SYSTEMS

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1T201	**ANALOG VLSI DESIGN**	**CORE**	4	0	0	4	4

Preamble: The Analog VLSI Design course focuses on developing the knowledge and analytical skills required for designing and analyzing CMOS analog circuits. The student will gain an indepth knowledge in the operation of MOS transistors, acquire the knowledge of the analysis and design of CMOS circuit including basic building blocks of CMOS circuits, amplifiers etc. The student will gain a glance in to the operation and design of advanced circuits.

Course Outcomes: After the completion of the course the student will be able to

CO 1	To the understand operation of MOSFET, IV Characteristics, small signal and large signal models and perform analysis
CO 2	Ability to analyze and design basic analog components including single stage amplifiers and current mirrors
CO 3	Ability to analyze and understand frequency response and noise sources in circuits
CO 4	Ability to design and analyze various single and multi stage operational amplifiers
CO 5	Gain understanding on the architecture and working of complex circuits such as PLL, comparators etc

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2				
CO 2	1	2	3			
CO 3	1	2		4		
CO 4	1	2	3			
CO 5	1	2		4	5	

Assessment Pattern

Course name	ANALOG VLSI DESIGN		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of whichstudent shall answer any five. Each question can carry 8 marks. Total duration of theexamination will be 3 Hrs.

Text Books

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata McGraw HILL, 2nd Edition 2015.
2. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.
3. R. Jacob Baker, CMOS circuit Design Layout and Simulation, 3rd Edition.
4. David. A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
5. Paul B Gray and Robert G Meyer, Analysis and Design of Analog Integrated Circuits 4th Edition.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lectures
1	**MOS Device Basics and Operation:**	
1.1	• MOS I/V Characteristics: Threshold voltage, derivation of I/V characteristics, regions of operation, MOS Transconductance.	1

1.2	• Second order effects: Body effect, Channel Length Modulation, Sub Threshold Conduction	1
1.3	• MOS Device Models: MOS device capacitances, MOS large signal model, MOS small signal model-basic, with channel length modulation, with body effect	2
1.4	• MOS Scaling Theory • MOS Short Channel Effects: Threshold Voltage Variation, Mobility degradation, velocity saturation, Hot carrier effects, Output impedance variation	1
2	**Basic MOS circuits:**	
2.1	• Single Stage Amplifiers: Common Source(CS) amplifier – Large signal and small signal behaviour with resistive load, diode connected load and current source load; CS amplifier with source degeneration • Source follower • Common gate stage	3
2.2	• Differential Amplifiers: Basic Differential Pair-large signal and small signal behaviour, Common Mode response • Differential Pair with MOS Loads	2
2.3	• Current Mirrors: Analysis and characteristics of Basic Current Mirror and Cascode Current Mirror • Active Current Mirrors: Differential pair(5 transistor OTA) with active load- large and small signal analysis	3
3	**Frequency response of circuits**	
3.1	• Frequency Response- Miller effect, bode plot, poles and zeroes, gain and phase margins , association of poles with nodes	2
3.2	• Analysis of common source amplifier frequency response • Analysis of common gate amplifier frequency response	3
3.3	• Analysis of frequency response of differential pair with active load	2
4	**Operational Amplifiers:**	
4.1	• Opamp Performance parameters • One stage op-amp topologies: characteristics and design of basic one stage opamp, telescopic cascode and folded cascode opamp	3
4.2	• Two stage Opamps: analysis and design of basic two stage topology and two stage telescopic cascode topology	2
4.3	• Common mode feedback (CMFB): basic concept • Common mode sensing in single stage opamp: (resistive feedback, source follower) • CMFB feedback techniques in single stage opamp	2
4.4	• Frequency compensation: need for compensation, Barkhausen's Criteria , root locus • Basic principle of compensation in a single stage telescopic cascode opamp • Miller compensation in two stage amplifier	3
5	**Advanced CMOS circuits:**	
5.1	• Temperature independent reference: Concepts and basic topology of positive temperature coefficient, negative temperature coefficient and bandgap reference	1
5.2	• Basic CMOS comparator: basic comparator circuit topology with pre-amplification, decision and output buffer stages [Reference book 3]	2
5.3	• Phase Locked Loops-Simple PLL(topology and dynamics), Charge pump PLL(topology and dynamics),	3
5.4	• MOS Sampling switches, resistance equivalence of parallel switched capacitor • Switched Capacitor unity gain buffer- basic topology and working • Non inverting Switched capacitor integrator - basic topology and working [Reference book 2]	4

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1T201**

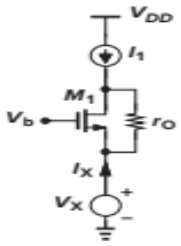
Course Name: **ANALOG VLSI DESIGN**

Max. Marks:60 Duration: 3 hours

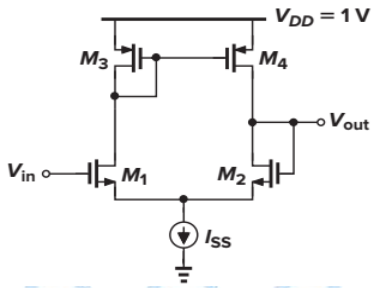
PART A

Answer all questions. Each question carries 4 marks.

1. With the help of a diagram explain the small signal model of a NMOS transistor considering the effect of channel length modulation and body effect
2. Analyze and compare the gain and output impedance of a common source amplifier with resistive load and an ideal current source load with the help of small signal models of the amplifiers.
3. Using millers theorem compute the input impedance of common gate amplifier shown in the figure below



4. Calculate the input common-mode voltage range and the closed-loop output impedance of the unity-gain buffer shown in the image below



5. With the help of diagrams explain the working of an XOR phase detector (PD). If the output swing is Vo, plot the input output characteristics of the PD. Calculate the gain of the XOR based PD from the output characteristics.

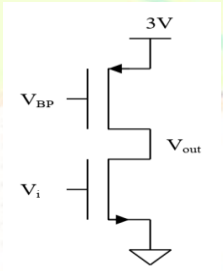
PART B

Answer any five questions. Each question carries 8 marks.

6. a) Consider a NMOS transistor with the parameters W/L = 100u/1u, with $\mu_n C_{ox}$ = 100uA/V_2, VDD = 3V, λ = 1/(10V), and V_{TH} = 1V. Carefully sketch by hand the drain current I_D vs. VDS. VDS has to swept from 0 to 3V at constant VGS=0, 1, 2, 3V. (calculations must be shown)

b) Consider a PMOS transistor with the parameters W/L = 100u/1u, with $\mu_p C_{ox}$ = 100uA/V_2, VDD = 3V, λ = 1/(10V), and V_{TH} = -1V. Carefully sketch by hand the drain current I_D vs. VDS. VDS has to swept from 0 to -3V at constant VGS = 0, -1, -2, -3 V. (calculations must be shown)

7. For a common source amplifier shown in figure below assume the following parameters: $\mu C_{ox}(W/L)$ =1mA/V_2 , |Vt|=1V, and λ = 0.1V_{-1} for both devices

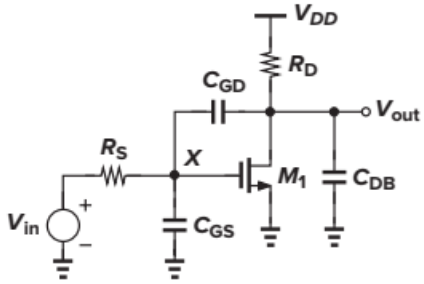


a) Assuming V_{BP} = 1.8 V, calculate V_{dsatp} and I_{dp} at V_{dp}=VDD-|V_{dsatp}| for the PMOS transistor.

b) Plot |I_{dp}| vs. Vout. What is the minimum and maximum value for Idp with the PMOS device in saturation in this circuit?

c) What is the value of Vi for which the NMOS device leaves saturation?

8. For a common source amplifier shown in figure estimate the input pole, output pole and transfer function of the circuit(use miller theorm)



9. Design a 2-stage NMOS input CMOS op-amp with the following specs:

- 200uA tail current
- able to sink 1mA from the load
- output swing to within 200mV of the rails
- input common mode range to within 200mV of the top rail, and 1.4V of the bottom rail.

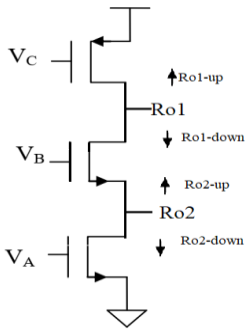
Process specs $\mu_n C_{ox}$ = 200uA/V2, $\mu_p C_{ox}$=100uA/V2, λ =1/(10V), Vthp = -1V, Vthn = 1V, VDD = 5V, Lmin = 0.5um, Oxide capacitance Cox=5fF/um2, Overlap capacitance Cov = 0.5fF/um. No ideal current sources are to be used in the design. The bias for the first stage tail must be generated using a current mirror with a resistive load.

Draw the schematic, label the device size of each transistor and the bias current flowing in each leg.

Calculate the 1st and 2nd stage gain, and the overall differential mode gain

10. Explain the concept for the generation of the negative and positive temperature coefficient sources with simple circuit diagram. Explain with the help of a circuit diagram how the positive and negative temperature confident sources can be combined to create and temperature independent voltage reference.

11. What is the low frequency impedance seen "looking up" and "looking down" at the output nodes Ro1 and Ro2 indicated in the circuit? Assume that all nmos devices have transconductance g_{mn} and output resistance r_{on}, and all pmos devices have transconductance g_{mp} and output resistance r_{op}. Write your answer in terms of g_{mp} , g_{mn}, r_{on}, and r_{op}. Write the full expression for up and down resistances Ro1-up, Ro1 -down, Ro2-up and Ro2-down. Use small signal models to derive the same.



12. For the PMOS-input folded cascode op-amp below, assume quadratic model and the following process specs $\mu_n C_{ox}$ = 250uA/V$_2$, $\mu_p C_{ox}$ = 125uA/V$_2$, λ = 1/(10V), Vtp = -0.2V, Vtn = 0.2V, Oxide Capacitance Cox = 5fF/um$_2$, Overlap capacitance Cov = 0.5fF/um

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1T202	**Sensor Technologies and MEMS**	Core	4	0	0	4	4

Preamble: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Understand the basic principles of sensors, signals, systems and the selection of a sensor for a particular application.
CO 2	Select, understand and design the various sensors for measuring different physical parameters.
CO 3	Select, understand and design the various sensors for measuring Chemical and Biological parameters.
CO 4	Design the signal conditioning circuits and interfacing electronics for sensors
CO 5	Design and understand the advanced micro sensors and MEMS

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	2	2	3	3	2	2
CO 2	2	2	3	3	2	2
CO 3	2	2	2	3	2	2
CO 4	2	2	3	3	2	2
CO 5	2	2	3	3	2	2

Assessment Pattern

	Sensor Technologies and MEMs		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	**Test 1 (% Marks)**
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project : 10 marks

Course based task/Seminar/Quiz : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (11 hours)

Data Acquisition: Sensors, Signals, and Systems, Sensor Classification. Sensor Characteristics: Static and Dynamic. Physical Principles of Sensing: Electric Charges, Fields, and Potentials, Capacitance, Induction, Resistance, Piezoelectric Effect, Hall Effect, Thermoelectric Effects.

MODULE 2 (11 hours)

Detectors of Humans, Presence, Displacement, Level, Force, Strain, Pressure and Flow.

MODULE 3 (8 hours)

Humidity and Moisture Sensors, Light Detectors, Temperature Sensors, Chemical and Biochemical Sensors.

MODULE 4 **(8 hours)**

Interface Electronic Circuits: Conditioning Bridge Circuits, Amplifiers for Signal Conditioning, Analog to Digital Converters for Signal Conditioning, Noise in Sensors and Circuits. Batteries for Low-Power Sensors, Signal Conditioning High Impedance Sensors.

MODULE 5 (7 hours)

An Introduction to MEMS: Micro-electromechanical Systems (MEMS) and micro systems, Definitions and Classifications, Applications, MEMS Fabrication Methods, Materials for Micromachining, Micro sensors and actuators. Smart sensors.

Reference Books

1) Jacob Fraden, "Handbook of Modern Sensors Physics, Designs, and Applications", Fifth Edition, Springer.
2) Tai-Ran Hsu, "MEMS and Microsystems design and manufacture", Tata McGraw Hill.
3) Jon S. Wilson," Sensor Technology Handbook", Elsevior.
4) Stoyan Nihtianov and Antonio Luque, "Smart Sensors and MEMS", Elsevior.
5) Murty D V S, "Transducers & Instrumentation", PHI, New Delhi

COURSE CONTENTS AND LECTURE SCHEDULE

(For 4 credit courses, the content can be for 45 hrs. and for 3 credit courses, the content can be for 36 hrs.)

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Data Acquisition: Sensors, Signals, and Systems, Sensor Classification	1
1.2	Sensor: Static Characteristics Dynamic	2
1.3	Sensor: Dynamic Characteristics	1
1.4	Physical Principles of Sensing: Electric Charges, Fields, and Potentials	1
1.5	Capacitor: Capacitance, Dielectric Constant	1
1.6	Induction: Lenz Law, Eddy Currents	1
1.7	Resistance: Specific Resistivity, Temperature Sensitivity of a Resistor, Strain Sensitivity of a Resistor, Moisture Sensitivity of a Resistor	1
1.8	Piezoelectric Effect: Ceramic Piezoelectric Materials, Polymer Piezoelectric Films	1
1.9	Hall Effect	1

1.10	Thermoelectric Effects: Seebeck Effect, Peltier Effect	1
	Module 2	
2.1	**Detectors of Humans** :Ultrasonic Detectors, Microwave Motion Detectors, Linear Optical Sensors	2
2.2	Optoelectronic Motion Detectors : Visible and Near-IR Light Motion Detectors , Passive Infrared (PIR) Motion Detectors	1
2.3	Optical Gesture Sensors	1
2.4	Tactile Sensors: Switch Sensors, Piezoelectric Tactile Sensors, Piezoresistive Tactile Sensors	1
2.5	Capacitive Touch Sensors, Optical Touch Sensors, Optical Fingerprint Sensors	1
2.6	Presence, Displacement, and Level: Potentiometric Sensors, LVDT and RVDT, Eddy Current Probes, Metal Detectors, Hall-Effect Sensors	2
2.7	Force and Strain: Strain Gauges, Pressure-Sensitive Films, Piezoelectric Force Sensors	1
2.8	Pressure Sensors: Bellows, Membranes, and Thin Plates, Piezoresistive Sensors, Vacuum Sensors, Ionization Gauges	1
2.9	Flow Sensors: Ultrasonic Sensors, Cantilever MEMS Sensors	1
	Module 3	
3.1	Humidity and Moisture Sensors: Capacitive Humidity Sensors, Resistive Humidity Sensors, Thermal Conductivity Sensor	2
3.2	Light Detectors: Photodiode, Phototransistor, Photoresistor, CCD and CMOS Imaging Sensors	2
3.3	Temperature Sensors: Resistance Temperature Detectors (RTD), Thermistors, Thermoelectric Sensors	2
3.4	Chemical Sensors, Biochemical Sensors, Conductometric Sensors, Metal Oxide Semiconductor (MOS) Chemical Sensors	2
	Module 4	
4.1	Signal Conditioners: Input Characteristics	1
4.2	Amplifiers: Operational Amplifiers, Voltage Follower, Charge- and Current-to-Voltage Converters, Light-to-Voltage Converters	2
4.3	Sensor Connections: Wheatstone Bridge, Bridge Amplifiers	1
4.4	Analog-to-Digital Converters, Successive-Approximation Converter	1
4.5	Signal Conditioning of high impedance sensors	1
4.6	Noise in Sensors and Circuits, Electric Shielding	1
4.7	Batteries for Low-Power Sensors, Energy Harvesting	1
	Module 5	
5.1	Micro-electromechanical Systems (MEMS) and micro systems	1
5.2	Definitions and Classifications, Applications	1
5.3	MEMS Fabrication Methods, Materials for Micromachining	1
5.4	Micro sensors: Bio sensors, Chemical, Optical, Pressure,	1

	Thermal	
5.5	Micro actuators: Micro Grippers, motors, valves and pumps	2
5.6	Smart sensors: Basic features	1

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: M24EC1T202
Course Name: Sensor Technologies and MEMS

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. State the relevance of different criteria for the selection of transducers for a particular application.
2. Illustrate the working of a Piezoresistive Tactile Sensors
3. Describe the basic principles of a CMOS imaging sensor
4. Explain any one method of energy harvesting
5. Explain with schematics the basic principle of a Micro gripper

PART B

Answer any five questions. Each question carries 8 marks.

6. a.How a first order sensor will respond to a step input. Explain with schematics
   b. With an example describe the piezoelectric effect. What are the different materials that exhibit piezoelectric effect.
7. a. Design an embedded system which will measure the angular displacement using LVDT.
   b. Show that a wire-wound resistance potentiometer can be used for measurement of linear and angular displacements.

8. a. Distinguish between photo-emissive, photo-conductive and Photo-voltaic cells and design one application for each.

   b. Design the signal conditioning circuit and block schematics of a thermistor based temperature controller switch.

9. a. With appropriate schematic analyze the working of Successive-Approximation A to D Converter

   b. Design a circuit to process the output of a strain gauge. Use Wheatstone bridge and instrumentation amplifier.

10. a. Design the circuits to interface a photo diode and photo conductive sensor.

    b. Explain the significance of noise in sensor. How electric shielding can be provided to regulate the noise.

11. a. Illustrate the block schematics of smart sensor and explain.

    b. With schematics describe the working and applications of a chemical micro sensor.

12. a. Elaborate on the basic principles of a MEMS and Micro system.

    b. With schematics describe the working and applications of a micro actuator.

Industry Integrated Course

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1S205	Embedded Hardware and Interfacing	Industry Course	3	0	0	3	3

Preamble: The objective of the course is to equip students with the knowledge and practical skills necessary to design, implement, and troubleshoot FPGA-based systems and control applications so as to make them ready for industry roles in technology and engineering.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Interface FPGAs with LEDs, buzzers, alphanumeric and graphical LCDs, optical and PIR sensors, and apply sensor interfacing and measurement techniques using A/D converters for measuring optical power, temperature, and strain (Blooms Level eg. Understand, Apply, Analyse)
CO 2	Interface and control relays, solenoid valves, and opto-isolators; interface and control DC, servo, BLDC, and stepper motors; implement liquid/fuel level control; perform voltage and current measurement; and interface and control power electronic devices
CO 3	Implement Discrete Fourier Transforms, design Digital Finite Impulse Response (FIR) filters, and design Digital Infinite Impulse Response (IIR) filters,
CO 4	Interface external SRAM, design basic memory controllers and implement ROM, single/dual port RAM
CO 5	Understand the operation of switching regulators and design a 12V Switched-Mode Power Supply (SMPS)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1		3	3	3	3
CO 2	1		3	3	3	3
CO 3	1		3	3	3	3
CO 4	1		3	3	3	3
CO 5	1		3	3	3	3

Assessment Pattern

Course name	Embedded Hardware and Interfacing		
Bloom's Category	**Continuous Internal Evaluation**		**End SemesterExamination (%Marks)**
	Test 1 (%Marks)	**Test 2 (%Marks)**	
Remember			
Understand	10	10	10

Apply	40	40	40
Analyse	50	50	50
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation

Seminar : 10 marks

Course based task/Seminar/Data collection and interpretation/Case study : 10marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

End Semester Examination

The examination will be for 3 Hrs and will contain 7 questions, with minimum one question from each module of which student should answer any five. Each question can carry 12 marks.

SYLLABUS

MODULE 1 (8 hours)

Interfacing of FPGA to I/O devices : Interfacing of FPGA to LED, Buzzer, Alphanumeric LCD, Graphical LCD, Optical sensors, and PIR sensors. Principles of Sensor Interfacing and Measurement Techniques, Interfacing of A/D converter and measurement Optical Power, Temperature and Strain.

MODULE 2 (8 hours)

FPGA Based Control : Interfacing Relay, Solenoid Valve and Opto-Isolator, DC Motor Interfacing and Control, Servo and BLDC Motor Interfacing and Control, Stepper Motor Control, Liquid/Fuel Level Control, Voltage and Current Measurement, Power Electronic Device Interfacing and Control.

MODULE 3 (8 hours)

Digital Signal Processing with FPGA : Discrete Fourier Transform, Digital Finite Impulse Response Filter Design, examples, Digital Infinite Impulse Response Filter Design, examples.

MODULE 4 (5 hours)

Interfacing of Memory devices to FPGA : External SRAM: Introduction, Specification of the IS61LV25616AL SRAM, Basic memory controller, a safe design. HDL templates for memory inference, Single port RAM, Dual port RAM, and ROM. Real-world examples

MODULE 5 (7 hours)

DC-DC converters for embedded boards : Switching regulators: Buck, Boost & Buck-boost – DCM ad CCM Operation, Waveforms – Selection of switches, filter inductance, and capacitance. Flyback converter: Operation, Waveforms, Design of a 12V SMPS adapter.

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Reference Books

1. A. Arockia Bazil Raj, "FPGA-Based Embedded System Developer's Guide", CRC Press.
2. Pong P. Chu, "FPGA Prototyping by Verilog Examples", John Wiley & Sons, 2008.
3. Shirshendu Roy, "Advanced Digital System Design", Springer
4. Wayne Wolf, 'FPGA-Based System Design' Pearson Education, 2004
5. Zhanyou Sha, Xiaojun Wang, "Optimal Design of Switching Power Supply", Wiley, 2015
6. L. Umanand, "Power Electronics: Essentials & Applications",Wiley

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1 (8 Hours)	
1.1	Interfacing of FPGA to LED, Buzzer	1
1.2	Alphanumeric LCD, Graphical LCD	3
1.3	Optical sensors, and PIR sensors. Principles of Sensor Interfacing and Measurement Techniques	2
1.4	Interfacing of A/D converter and measurement Optical Power, Temperature and Strain	2
	Module 2 (8 Hours)	
2.1	Interfacing Relay, Solenoid Valve and Opto-Isolator	2
2.2	DC Motor Interfacing and Control	1
2.3	Servo and BLDC Motor Interfacing and Control	2
2.4	Stepper Motor Control	1
2.5	Liquid/Fuel Level Control, Voltage and Current Measurement	1
2.6	Power Electronic Device Interfacing and Control	1
	Module 3 (8 Hours)	
3.1	Digital Signal Processing with FPGA : Discrete Fourier Transform	3
3.2	Digital Finite Impulse Response Filter Design, examples	3
3.3	Digital Infinite Impulse Response Filter Design, examples	2
	Module 4 (5 Hours)	
4.1	Interfacing of Memory devices to FPGA : External SRAM: Introduction, Specification of the IS61LV25616AL SRAM,	1
4.2	Basic memory controller, a safe design.	2
4.3	HDL templates for memory inference, Single port RAM, Dual port RAM, and ROM. Real-world examples	2
	Module 5 (7 Hours)	
5.1	DC-DC converters for embedded boards : Switching regulators: Buck, Boost & Buck-boost – DCM ad CCM Operation, Waveforms – Selection of switches, filter inductance, and capacitance.	3

5.2	Flyback converter: Operation, Waveforms	2
5.3	Design of a 12V SMPS adapter.	2

Model Question Paper

QP CODE: Pages: X

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

SECOND SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: M24EC1S205

Course Name: Embedded Hardware and Interfacing

Max. Marks:60 Duration: 3 hours

Answer any five questions. Each question carries 12 marks.

1. Develop a digital system in the FPGA to display the total number of persons present in an auditorium using two PIR sensors. The system design has to be as follows.
   i. The PIR sensor module is installed at entry and exit.
   ii. ii. Person entry as well as exit have to be counted independently.
   iii. iii. The total number of persons present in the room has to be displayed on a two digit seven-segment display. Therefore, the display may vary from 00 to 99.

2. In an R/2R ladder DAC circuit, feedback is designed with 1-KΩ (connected between an inverting terminal and ground) and 7-KΩ (connected between an inverting terminal and output [Vo] of an operational amplifier) resistors. A four-stage R/2R ladder circuit is connected to the noninverting terminal. Find the Vo when the binary input is “1010”.

3. Assume that an optical sensor output voltage is connected to the noninverting terminals of op-amps (LM324). Using this circuit, design a 2-bit A/D converter to get the possible binary outputs for the different values of sensor output voltages.

4. Develop a Verilog code of SRAM controller.

5. With the help of waveforms, explain the working of a Flyback converter.

6. Develop a digital system in the FPGA to realize a FIR filter. The impulse response h[n] of the filter is {−2, −1, 3, 4}. Get signed input samples of width 8 from the eight GPIO pins.

7. Write a Verilog code to implement (i) A single port RAM (ii) Dual Port RAM (iii) ROM

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1P206	MINI PROJECT	PROJECT	0	0	3	3	3

Mini project can help to strengthen the understanding of student's fundamentals through application of theoretical concepts and to boost their skills and widen the horizon of their thinking. The ultimate aim of an engineering student is to resolve a problem by applying theoretical knowledge. Doing more projects increases problem solving skills.

The introduction of mini projects ensures preparedness of students to undertake dissertation. Students should identify a topic of interest in consultation with PG Programme Coordinator that should lead to their dissertation/research project. Demonstrate the novelty of the project through the results and outputs.The progress of the mini project is evaluated based on three reviews, two interim reviews and a final review. A report is required at the end of the semester.

Evaluation Committee - Programme Coordinator, One Senior Professor and Guide.

Sl. No.	Type of evaluations	Mark	Evaluation criteria
1	Interim evaluation 1	20	
2	Interim evaluation 2	20	
3	Final evaluation by a Committee	35	Will be evaluating the level of completion and demonstration of functionality/ specifications, clarity of presentation, oral examination, work knowledge and involvement
4	Report	15	The committee will be evaluating for the technical content, adequacy of references, templates followed and permitted plagiarism level(not more than 25%)
5	Supervisor/Guide	10	
	Total	100	

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1L207	Advanced Microcontroller Lab	Laboratory	0	0	3	2	2

Preamble: This laboratory course will allow students to get in-depth knowledge in Embedded Systems and programming. Students will be able to interface various peripherals to ARM Cortex-based Microcontroller.

Prerequisite: Knowledge of any basic microcontroller and programming.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Gain Knowledge about the architectural features and instructions of 32 bit ARM microcontroller.
CO 2	Understand the selection of programming language and embedded C
CO 3	Understand the basic hardware components and their selection in the design of an Embedded System.
CO4	Understand various Sensors, Actuators & Interfacing Modules.
CO 5	Students must be able to design and implement an embedded system to meet the requirements of real time application.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1		1	2	2	2
CO 2	1		1	2	2	2
CO 3	1		1	2	2	2
CO 4	2		1	2	2	3
CO 5	3	1	1	2	2	3

Mark distribution

Total Marks	CIE Marks
100	100

Continuous Internal Evaluation Pattern:

Lab work and Viva-voce : 60 marks
Final assessment Test and Viva voce : 40 marks

The laboratory courses will be having only Continuous Internal Evaluation and carries 100 marks. Final assessment shall be done by two examiners; one examiner will be a senior faculty from the same department.

SYLLABUS

LIST OF EXPERIMENTS

1	LED blinking using software delay loop.
2	LED blinking using timer module.
3	Control of LED using an input switch.
4	Display seconds on the 7-segment module from RTC.
5	Display seconds (two digits) on two 7-segment displays from RTC using multiplexing.
6	Display characters sent from the microcontroller on a PC.
7	Create a voltage divider using a potentiometer and read and display the voltage across the potentiometer using ADC and DAC.
8	Transmit a character from PC to microcontroller and display an LED if the transmitted character is – "&".
9	Generate a sine wave using a DAC module. Use a lookup table to store the sine table.
10	Generate a sine wave of frequency 200Hz or 500Hz. Use a switch to select the frequency.
11	Generate a square wave using the PWM module and control its duty cycle.
12	Implement SPI communication by transmitting 8-bit data by the master and receive it using SPI slave.

Reference books

1. Noviello, Carmine. "Mastering STM32."
2. Norris, Donald. Programming with STM32: Getting Started with the Nucleo Board and C/C++. McGraw Hill Professional, 2018.

SEMESTER II
PROGRAM ELECTIVE III

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E203A	**Embedded Networking**	Program Elective 3	3	0	0	3	3

Preamble: The purpose of this course is to provide a solid foundation that furnishes the learner with in-depth knowledge of embedded networks. Students will get an overall idea regarding the protocols used in embedded systems and real-time embedded systems. The syllabus covers basic protocols like UART and very advanced real-time protocols like CAN. This course helps the learner to design an embedded system with various interfaces to I/O devices and peripherals as per the requirement and implement it with a professional grade.

Prerequisite: Knowledge of any microcontroller and its serial interfaces.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Study the basic embedded protocols like UART and practical networks like RS232 and RS485. **(Cognitive Knowledge Level: apply, Analyse and create)**
CO 2	Study and design the basic embedded networks with popular protocols like SPI and I2C **(Cognitive Knowledge Level: apply, Analyse and create)**
CO 3	Study a real time industrial grade embedded network CAN and try design a real time implementation with it. **(Cognitive Knowledge Level: apply and Analyse)**
CO 4	The most widely used network is based on LAN technologies. Student will be able to study and create networks in LAN. **(Cognitive Knowledge Level: Apply and analyse)**
CO 5	Mobile hand sets and laptops are widely connected by wireless technologies. Students will be able understand and create networks based on wireless technologies. **(Cognitive Knowledge Level: apply, Analyse and create)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyse and solve practical engineering problems.s
PO 6	An ability to engage in life-long learning for the design and development of the stream related problems taking into consideration sustainability, societal, ethical and environmental aspects. Also to develop cognitive skills for project management and finance which focus on Industry and Entrepreneurship.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	2	1	2	2	2	2
CO 2	2	1	2	2	2	2
CO 3	2	1	2	2	2	2
CO 4	2	1	2	2	2	2
CO 5	2	1	2	2	2	2

Assessment Pattern

	M242E1EC31- Embedded Networking		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	**CIE marks**	**ESE marks**	**ESE Duration**
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project : 10 marks

Course based task/Seminar/Quiz : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through

long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of theexamination will be 3 Hrs.

SYLLABUS

MODULE 1: **Introduction (7 Hrs)**

Embedded Networking Requirements: Introduction to Network for Embedded Systems, Serial/Parallel Communication, Synchronous/Asynchronous Serial Protocols,
Serial communication protocols -UART, RS232, RS485.

MODULE 2: **SPI and I2C (7 Hrs)**

SPI : Introduction, Features, Modes of Operation , External Signal Description, Functional Description(Covering Master Mode, Slave Mode, Transmission Formats, Baud Rate Generation, Error Conditions, Low Power Mode Options)
I2C : I2C-bus features, Modes of Operation - Standard-mode, Fast-mode, Fast-mode plus, Ultra fast mode. Signals and Logic levels, Start/Stop conditions, byte format, Acknowledge and Not-Acknowledge, Clock Synchronization, Arbitration, Clock Stretching, Addressing, Call Addresses, Reset, Device ID, Applications of I2C bus protocol.

MODULE 3 : **CAN Controller (7 Hrs)**

Controller Area Network : CAN Overview, Introduction, CAN 2.0b Standard. Physical Layer, Message Frame Formats, Bus Arbitration, Message Reception and Filtering, Error Management, Selecting a CAN Controller, CAN Development Tools.

MODULE 4 : LAN (7 Hrs)

Elements of a LAN- Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed. OSI reference model, TCP/IP reference model.
IP addressing, Subnetting.

TCP/IP: Introduction to TCP/IP: History, Architecture -layering, Standards and Applications, Protocol Overview, Routers & Topology, IP routing, TCP Architecture, UDP Architecture, Security Concepts.

MODULE 5 : Wireless Network (8 Hrs)

Wireless networks: Wifi - 802.11 standards, Architecture and protocol stack, Physical layer, MAC sublayer, 802.11 frame structure.
Bluetooth - Architecture, protocol stack - radio layer, link layers, frame structure. Frequency hopping, piconets and scatternets.
Networking Examples - Home Automation. Block diagram, schematic, and remote control using IoT

Text Books

1. ANDREW S. TANENBAUM, "COMPUTER NETWORKS", FIFTH EDITION, Pearson Education, Inc., publishing as Prentice Hall. 2011
2. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 2008.
3. Lyla B Das, “Embedded Systems-An Integrated Approach”, Pearson, 2012.
4. Olaf P Feiffer, Andrew Ayre & Christian Keyold, “Embedded Networking with CAN and CAN Open”, Embedded System Academy, 2005.
5. Marco Di Natale, Haibo Zeng, Paolo Giusto & Arakadeb Ghosal, “Understanding and Using the Controller Area Network”, Springer, 2012.
6. John Catsoulis, "Designing Embedded Hardware", O'Reilly Media, Inc., 2002.
7. Dr. Sidnie Feit, “TCP/IP: Architectures, Protocols and Implementations with IPv6 and IP Security”, Tata McGraw Hill, Second Edition, 2008.
8. Martin W. Murhammer, Orcun Atakan, Stefan Bretz, Larry R. Pugh, Kazunari Suzuki, David H. Wood, “TCP/IP Tutorial and Technical Overview”, International Technical Support Organization-IBM, Sixth Edition, October 1998.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Introduction - Embedded Networking	1
1.2	Serial/Parallel Communication	2
1.3	Synchronous/Asynchronous Serial Protocols	3
1.4	UART	4
1.5	RS232	5
1.6	RS485	6
	Module 2	
2.1	SPI: Introduction, Features	1
2.2	Modes of Operation, External Signal Description	2
2.3	Master Mode, Slave Mode	3
2.4	Transmission Formats, Baud Rate Generation, Error Conditions, Low Power Mode	4
2.5	I2C : I2C-bus features, Modes of Operation - Standard-mode, Fast-mode, Fast-mode plus, Ultra fast mode.	5
2.6	Signals and Logic levels, Start/Stop conditions, byte format, Acknowledge and Not-Acknowledge	6
2.7	Arbitration, Clock Stretching, Addressing, Call Addresses, Reset, Device ID	7
2.8	Applications of I2C bus protocol.	8
	Module 3	

3.1	Controller Area Network : CAN Overview, Introduction, CAN 2.0b Standard.	1
3.2	Physical Layer, Message Frame Formats	2
3.3	Bus Arbitration, Message Reception and Filtering	3
3.4	Error Management	4
3.5	Selecting a CAN Controller	5
3.6	CAN Development Tools.	6
	Module 4	
4.1	Elements of a LAN- Inside Ethernet – Building a Network	1
4.2	Hardware options – Cables, Connections and network speed.	2
4.3	OSI reference model	3
4.4	TCP/IP reference model, IP addressing, Subnetting.	4
4.5	TCP/IP: Introduction to TCP/IP: History, Architecture	5
4.6	TCP/IP -layering	6
4.7	Protocol Overview, Routers & Topology, IP routing	7
4.8	TCP Architecture, UDP Architecture,	8
4.9	Standards and Applications, Security Concepts.	9
	Module 5	
5.1	Wireless networks: Wifi - 802.11 standards	1
5.2	Architecture and protocol stack, Physical layer, MAC sublayer	2
5.3	802.11 frame structure.	3
5.4	Bluetooth - Architecture	4
5.5	Bluetooth - protocol stack - radio layer, link layers,	5
5.6	Bluetooth - frame structure. Frequency hopping, piconets and scatternets.	6
5.7	Networking Examples - Home Automation. Block diagram, schematic, and remote control using IoT.	7

CO ASSESSMENT QUESTIONS

Course Outcome 1 (CO1):

1. What are the significance of UART, RS232 and RS485 protocols in the embedded communication?
2. What is the protocol used UART, RS232 and RS485 protocols in the embedded communication?
3. How a practical network can be configured for UART, RS232 and RS485? Demonstrate with an application

Course Outcome 2 (CO2):

1. What are the significance and features of SPI and I2C protocols in the embedded communication?
2. Draw the timing diagram for SPI and I2C for Read, write, acknowledgement and multibyte transmission.
3. Design a practical network for SPI and I2C? Demonstrate with an application.

Course Outcome 3 (CO3):

1. What are the significance and features of CAN protocols in the embedded communication?
2. Why it is called as industrial-grade network?
3. Draw the timing diagram for CAN and illustrate arbitration.
4. Design a practical network for CAN and explain it with an application

Course Outcome 4 (CO4):

1. What are the significance of LAN and ethernet protocols in the embedded communication?
2. Draw the protocol stack for Ethernet and TCP/IP.
3. How a practical network can be configured using IP addressing, show how the subnetting can be used effectively for the formation of networks.

Course Outcome 5 (CO5):

1. What are the significance of WiFi and Bluetooth protocols in the embedded communication?
2. Draw the protocol stack for WiFi and Bluetooth.
3. How a practical network can be configured using IP addressing in wireless networks, show how the subnetting can be used effectively for the formation of networks.
4. Show how a Bluetooth network is for practical applications.

Model Question paper

QP CODE: **PAGES: 2**

Reg No: **Name:**

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM
FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: M24EC1E203A

Course Name: Embedded Networking

Max. Marks: 60 **Duration: 3 Hours**

PART A
Answer all Questions. Each question carries 4 Marks

1. What is the use of parity in communication? How odd and even parities are calculated?
2. Draw the standard CAN frame and mark various fields. Calculate the size of a CAN frame if the size of the data is 7 bytes and the identifier is 11bits.
3. What are the signal levels in the idle lines of I2C? Explain the S and P conditions of the I2C communication.
4. An organization with 4 departments has the following IP address space: 11.3.22.0/23. It is required to create subnets to accommodate 4 departments. The subnets have to support to a minimum of 220, 64, 50, and 23 hosts respectively. What are the 4 subnet network numbers?
5. Consider the following loops, identify the true dependencies, output dependences and anti-dependences and eliminate the output dependences and anti-dependences. **(5x4=20 Marks)**

PART B
Answer any 5 questions. Each question carries 8 marks

6. Calculate the bandwidth usage for CAN network with SYNC cycle time 33ms, Data length per message is 22 bytes and bus speed is 125kbps.

7. How synchronization is achieved in CAN communication? The following data is to be sent over the CAN bus. Show the timing diagram after the bit stuffing. 11000001111000011110.
8. In I2C bus what are the importance of ACK and NACK conditions? What are the conditions which generate a NACK status?
9. Draw frame format for IEEE802.3 LAN packet format. Calculate maximum and minimum size of a frame.
10. What is frequency hopping and paging in Bluetooth?
11. An organization with 4 departments has the following IP address space: 11.3.22.0/23. It is required to create subnets to accommodate 4 departments. The subnets have to support to a minimum of 220, 64, 50, and 23 hosts respectively. What are the 4 subnet network numbers?

(5x8=40 Marks)

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E203B	SOC DESIGN	PROGRAMME ELECTIVE III	3	0	0	3	3

Preamble : Systems-on-Chip (SoCs) are at the core of most embedded computing and consumer devices. As a result, SoCs represent the fastest-growing segment of the semiconductor industry.The purpose of this course is to provide a solid foundation on System-on-Chips (SoCs) where many functions of an electronic system are integrated into a single chip. This course helps the learner to understand different components and design abstractions that contribute towards building complex systems, and apply this understanding to improve state-of-the-art System-on-Chip (SoC) designs. At the end of this program, a student would be able to appreciate and apply advances made across domains to design better SoCs.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Study components of System on chip and its architecture. (Cognitive Knowledge Level: Analyse)
CO 2	Study System on chip design process, system level design issues and the concept of design reuse. (Cognitive Knowledge Level: Analyse)
CO 3	Study hard macro design process, familiarize with RTL coding guidelines and macro synthesis guidelines. Use the knowledge gained to design various systems. (Cognitive Knowledge Level: Apply)
CO 4	Study Verification technology options, methodologies, and get familiarized with the SoC verification flow. Use the knowledge gained to design Testbenches for verification. (Cognitive Knowledge Level: Apply)
CO 5	Study MPSoCs, Techniques for designing MPSoC and understand the overview of SoC design flow with detailed application study. (Cognitive Knowledge Level: Analyse)
CO 6	Design and verification of SoC (Cognitive Knowledge Level: Create)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2				
CO 2	1	2				
CO 3	1		3			
CO 4	1		3			
CO 5	1	2		4	5	

Assessment Pattern

Course name	SoC DESIGN		
Bloom's Category	**Continuous Internal Evaluation**		**End SemesterExamination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	

Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application,analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Introduction to the Systems Approach

System Architecture, Components of the System, Hardware and Software,Processor Architectures, Memory and Addressing, SystemLevel Interconnection,System Architecture and Complexity, Product Economics and Implications for SOC, Dealing with Design Complexity.

MODULE 2 (8 hours)

Design for reuse, System On Chip Design Process

A canonical SoC Design, SoC,Design flow - waterfall vs. Spiral,Top-down vs. Bottom up, Specification requirement, Types of Specification,System Design process, System level design issues- Soft IP vs. Hard IP,Design for timing closure, Logic design issues, Physical design issues,Macro Design Process- Overview, Key features, Planning and specification,Macro design and verification, Soft Macro productization.

MODULE 3 (8 hours)

Developing hard macros

Design issues for hard macros, Design process, System Integration with reusable macros, RTL Coding Guidelines: Basic Coding Practices, Coding for Portability ,Coding for Synthesis. Macro Synthesis Guidelines

MODULE 4 **(8 hours)**

SoC Verification

Verification technology options, Verification methodology,Verification approaches, System level verification,Block level verification, Hardware/software co-verification - Co-verification Environment,Macro Verification Guidelines-Verification Plan, Verification Strategy,Testbench Design, Timing Verification

MODULE 5 **(8 hours)**

What, Why, How MPSoCs, Techniques for designing energyaware MPSoCs- Energy-Aware Processor Design ,Energy-Aware Memory System Design, Energy-Aware OnChip Communication System Design ,MPSoC performance modeling and analysis,SoC Design Approach and application study

Text Books

1. Computer System Design: System-on-Chip; Michael J. Flynn, Wayne Luk , ISBN: 978-1-118-00991-8 August 2011
2. Reuse Methodology Manual for System-On-A-Chip Designs, Springer, 32nd Edition, 2007
3. System-on-a-Chip Verification - Methodology and Techniques; Prakash Rashinkar, Peter Paterson, Leena Singh; 2002, Kluwer Academic Publishers
4. Jerraya, W.Wolf, Multiprocessor Systems-on-chips, M K Publishers.
5. RochitRajsuman, "System-on-a-chip: Design and Test ", Artech House, 2000 ISBN
6. Dirk Jansen,The EDA HandBook, Kluwer Academic Publishers.
7. William K.Lam, Design Verification: Simulation and Formal Method based Approaches,Prentice Hall.
8. Modern System-on-Chip Design on Arm; DAVID J. GREAVES, ARM Education Media, 20

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Introduction to the Systems Approach	
1.1	System Architecture, Components of the System, Hardware and Software	2
1.2	Processor Architectures, Memory and Addressing, System Level Interconnection	3
1.3	System Architecture and Complexity, Product Economics and Implications for SOC, Dealing with Design Complexity	3
	Design for reuse, System On Chip Design Process	
2.1	A canonical SoC Design, SoC,Design flow - waterfall vs. spiral	1
2.2	Top-down vs. Bottom up, Specification requirement, Types of Specification	1
2.3	System Design process, System level design issues- Soft IP vs. Hard IP	2
2.4	Design for timing closure, Logic design issues, Physical design issues	2
2.5	Macro Design Process- Overview, Key features, Planning and specification	1
2.6	Macro design and verification, Soft Macro productization	1
	Developing hard macros	
3.1	Design issues for hard macros, Design process	2
3.2	System Integration with reusable macros	2
3.3	RTL Coding Guidelines: Basic Coding Practices, Coding for Portability	2
3.4	Coding for Synthesis. Macro Synthesis Guidelines	2
	SoC Verification	
4.1	Verification technology options, Verification methodology	2
4.2	Verification approaches, System level verification	2
4.3	Block level verification, Hardware/software co-verification - Co-verification Environment	2
4.4	Macro Verification Guidelines-Verification Plan, Verification Strategy	1
4.5	Testbench Design, Timing Verification	1
	MPSoCs	
5.1	What, Why, How MPSoCs, Techniques for designing energyaware MPSoCs- Energy-Aware Processor Design	2
5.2	Energy-Aware Memory System Design, Energy-Aware OnChip Communication System Design	2
5.3	MPSoC performance modeling and analysis.	2
5.4	SoC Design Approach and application study	2

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E203B**

Course Name: **System on chip design**

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

8. Differentiate between VLIW and Superscalar processors.
9. Specify the need of using reusable IP core and differentiate between Hard IP and Soft IP.
10. Explain briefly the design issues for hard macro.
11. Briefly explain block level verification and stress on its need.
12. What are the techniques used for controlling the power consumption of MPSoC.

PART B

Answer any five questions. Each question carries 8 marks.

6. Compare SOC interconnect methods.
7. Give a brief account of the logic design issues faced when designing for timing closure.
8. Design a 4 bit up-down counter using VHDL and verify the functionality using a Testbench
9. Briefly explain the characteristics of a good IP.What are the main challenges faced while Integrating macros into the SoC design and explain the strategies for dealing with them?
10. You are required to develop a Set-Top Box SoC which inputs a signal and transforms the data to content displayed on a TV screen. The target feature size is at the 65nm technology node. The Set-Top Box SoC architecture must consist of the following components: 64b CISC processor with 48KB of I-cache and 32KB of D-cache, A Texas Instrument DSP (for video signal acquisition), A SHARC-based DSP (for demodulation/ error correction schemes), MPEG-2 transport stream demultiplexer accelerator unit, Bus and bus control, Application Memory (512KB), Shared SRAM L2 cache.Design an SoC based on the given specifications and also mention the SoC design flow.
11. Differentiate between Formal Model checking and Equivalence checking.
12. In the definition phase of a SoC architecture, a number of technical factors are considered for the implementation and mapping of the appropriate algorithms. Describe in detail with an application such as a 3 - D graphics engine, the factors you would consider essential for achieving your go

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E203C	VLSI STRUCTURE FOR DSP	PROGRAM ELECTIVE III	3	0	0	3	3

Preamble: The purpose of this course is to introduce students to the fundamentals of VLSI signal processing and applications. The Course describes the design and optimization of VLSI architectures for basic DSP algorithms.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Study the fundamentals of Pipelining.
CO 2	Evaluate parallel architectures useful in DSP implementation.
CO 3	Apply Pipelining and Parallel processing of IIR systems.
CO 4	Analyse fast convolution methods
CO 5	Understand Scaling and round off noise in filters.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1		2	2		
CO 2	1		3	3		
CO 3	1		3	4		
CO 4	1		3	4		
CO 5	1		3	4		

Assessment Pattern

Course name	VLSI STRUCTURE FOR DSP		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application,analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Review of Pipelining and parallel processing for FIR filters, algorithmic strength reduction-introduction, parallel FIR filters, Discrete Cosine Transform and inverse DCT

MODULE 2 (8 hours)

Implementation of DCT and inverse DCT based on algorithm-architecture transformations.

Parallel architectures for Rank Order filters - Odd Even Merge sort architecture-Rank Order filter architecture-Parallel Rank Order filters-Running Order Merge Order Sorter-Low power Rank Order filter.

MODULE 3 (8 hours)

Pipelined and parallel recursive filters, Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

MODULE 4 (8 hours)

Fast convolution: Introduction, Cook-Toom Algorithm, Modified Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution, cyclic convolution.

MODULE 5 (8 hours)

Scaling and round off noise - Round off noise in pipelined IIR filters – round off noise in lattice filters, pipelining of lattice IIR digital filters – low power CMOS lattice IIR filters

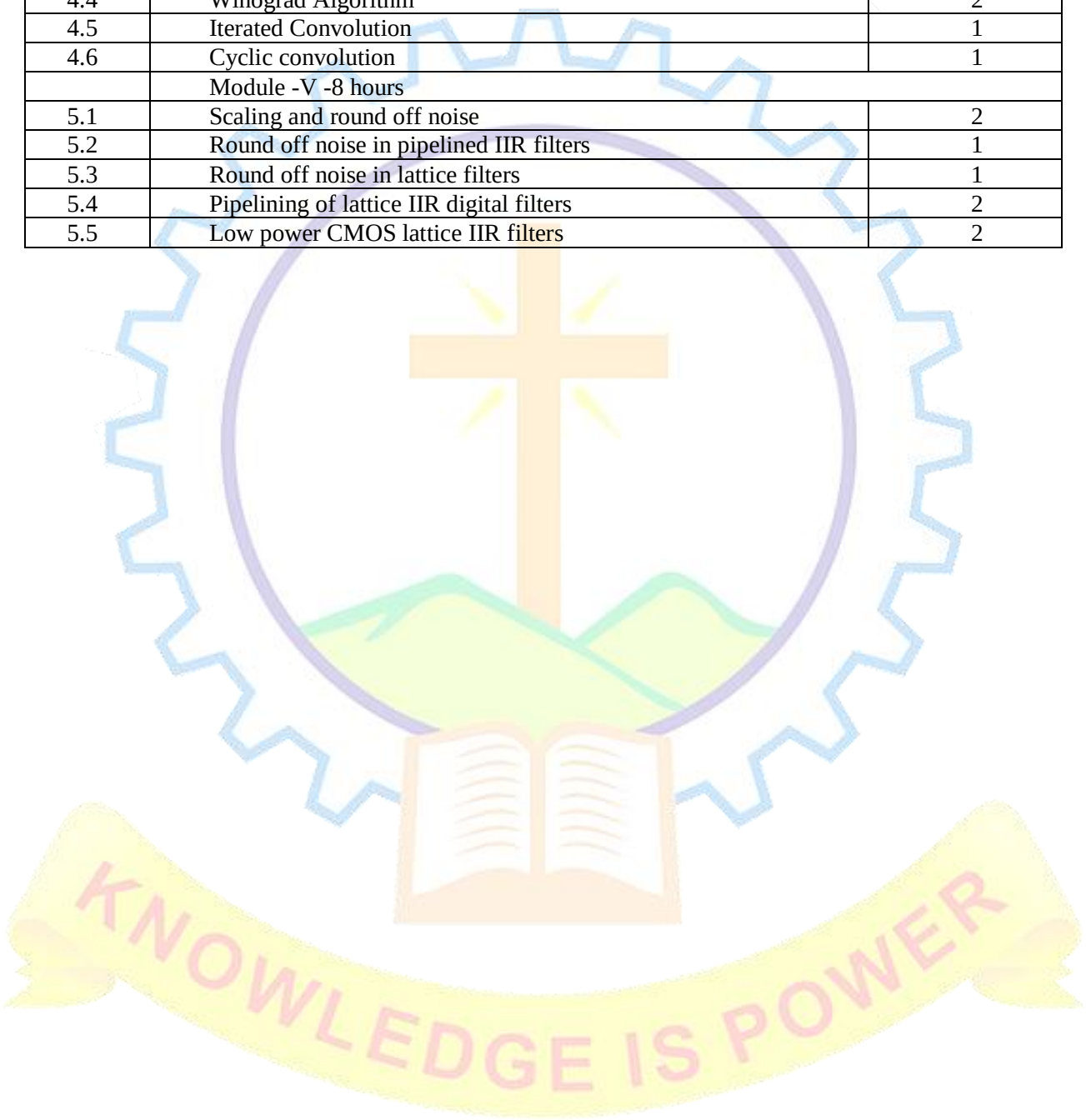
Text Books

1. Keshab K. Parhi, VLSI Digital signal processing Systems: Design and Implementation, John Wiley & Sons, 1999.
2. Uwe meyer- Baes, DSP with Field programmable gate arrays, Springer, 2001
3. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill, 1994.
4. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern singal processing, Prentice Hall, 1985.
5. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall, 1994.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
1	Module 1-8 hours	
1.1	Review of Pipelining and parallel processing for FIR filters	2
1.2	Algorithmic strength reduction-introduction	2
1.3	parallel FIR filters	1
1.4	Discrete Cosine Transform	2
1.5	Inverse DCT	1
2	Module-II -8 hours	
2.1	Implementation of DCT and inverse DCT based on algorithm-architecture transformations.	2
2.2	Parallel architectures for Rank Order filters	1
2.3	Odd Even Merge sort architecture	1
2.4	Rank Order filter architecture	1
2.5	Parallel Rank Order filters	1
2.6	Running Order Merge Order Sorter	1
2.7	Low power Rank Order filter	1
	Module-III -8 hours	
3.1	Pipelined and parallel recursive filters	1
3.2	Look-Ahead pipelining in first-order IIR filters	1
3.3	Look-Ahead pipelining with power-of-2 decomposition	1
3.4	Clustered look-ahead pipelining	1
3.5	Parallel processing of IIR filters	2

3.6	Combined pipelining and parallel processing of IIR filters.	2
	Module-IV -8 hours	
4.1	Fast convolution: Introduction	1
4.2	Cook-Toom Algorithm	2
4.3	Modified Cook-Toom Algorithm	1
4.4	Winograd Algorithm	2
4.5	Iterated Convolution	1
4.6	Cyclic convolution	1
	Module -V -8 hours	
5.1	Scaling and round off noise	2
5.2	Round off noise in pipelined IIR filters	1
5.3	Round off noise in lattice filters	1
5.4	Pipelining of lattice IIR digital filters	2
5.5	Low power CMOS lattice IIR filters	2



Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E203C**

Course Name: **VLSI STRUCTURE FOR DSP**

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. How transpose of a matrix in 2x2 linear convolution algorithm can be used to obtain the 2 parallel filter.
2. Obtain the structure of time mapped rank order filter with W=8.
3. Write short notes on low power CMOS lattice IIR filters.
4. Obtain the matrix form of traditional 2 parallel FIR filter and draw its structure.
5. Explain Clustered look-ahead pipelining.

PART B

Answer any five questions. Each question carries 8 marks.

6. State three steps of Algorithm-Architecture transformation. Prove that this method effectively reduces the number of multiplications in the implementation of 8-point DCT.

7. Consider the first order IIR filter with transfer function.

$H(Z) = 1/ (1 – az^{-1})$. Derive the filter structure with 4 level pipelining and 3 level block Processing.

8. Consider the odd-even merge based rank order filter with window size W=5. Assume that the filter is to be pipelined and total capacitance for one C&S unit to be Co. a) What is the power consumption of a 3 parallel filter. b) What is the power consumption with substrate sharing implementation.

9. Consider a 2x3 linear convolution s(p)=h(p)x(p). where h(p)=h0+h1p, x(p)=x0+x1p+x2 p2. Use Cook Toom algorithm to construct an efficient implementation for the given linear convolution.

10. Explain how round off noise is calculated in lattice filters and IIR filters.

11. Construct a 3 x 3 convolution using a 4 x 4 cyclic convolution algorithm.

12. Derive Fast 2m-point DCT structure by the decimation-in-frequency approach.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E203D	SEMICONDUCTOR MEMORIES	PROGRAM ELECTIVE III	3	0	0	3	3

Preamble: This course aims to impart the advance knowledge of memory devices and enable students to Design, test and debug the memory devices.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Analyse the different types of RAM and ROM design
CO 2	Analyse the different RAM and ROM architecture and interconnect
CO 3	Analyse about design and characterization techniques.
CO 4	Analysis of different memory testing and design for testability.
CO 5	Identification of new developments in semiconductor memory design

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1			2			
CO 2			3		5	
CO 3	1		3	4	5	
CO 4	1		3	4	5	
CO 5			3			

Assessment Pattern

Course name	SEMICONDUCTOR MEMORIES		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application,analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of whichstudent shall answer any five. Each question can carry 8 marks. Total duration of theexamination will be 3 Hrs.

SYLLABUS

MODULE 1 (9 hours)

Random Access Memory Technologies: Static Random Access Memories (SRAMs):SRAM cell structure MOS SRAM architecture, MOS SRAM cell and peripheral circuit operation, bipolar SRAM technologies, silicon on insulator (SOI) technology, advanced SRAM architectures and technologies, application specific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM technology development, CMOS CRAMs, DRAMs cell theory and advanced cell structures- BiCMOS DRAMs-soft error failure in DRAMs, Advanced DRAM designs and architecture, application specific DRAMs.

MODULE 2 (9 hours)

Non-volatile Memories: Masked Read only memories (ROMs): High density ROMs, programmable read-only

memories (PROMs)- bipolar PROMs, CMOS PROMs, erasable (UV)- Programmable read-only memories (EPROMs)- Floating Gate EPROM cell- one, time programmable (OTP) Eproms, Electrically Erasable PROMs (EEPROMs), EEPROM technology and architecture, non-volatile SRAM-Flash memories (EPROMs or EEPROM), Advanced flash memory architecture.

MODULE 3 (7 hours)

Memory fault modelling, testing and memory design for Testability and fault tolerance, RAM fault modelling, electrical testing, Pseudo random testing, megabit DRAM testing non-volatile memory modelling and testing, IDDQ fault modelling and testing, application specific memory testing.

MODULE 4 **(7 hours)**

Semiconductor memory reliability: General Reliability issues, RAM failure modes and mechanism, non volatile memory reliability, reliability modelling and failure rate prediction, design for reliability, reliability test structures, reliability screening and qualification.

MODULE 5 (8 hours)

Advanced memory technologies and high-density memory packaging technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog memories, magneto resistive random access memories (MRAMs), Experimental memory devices. Memory hybrids and MCMs (2D), Memory stacks and MCMs (3D), Memory MCM testing and reliability issues- memory cards-high density memory packaging future directions.

Text Books

1. Ashok K.Sharma, Semiconductor Memories Technology, testing and reliability, Prentice hall of India Private Limited, New Delhi 1997.
2. Ashok K Sharna, Advanced Semiconductor Memories – Architecture, Design and Applications, Wiley 2002.
3. Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1 : **Random Access Memory Technologies**	
1.1	**(SRAMs)**: SRAM cell structure MOS SRAM architecture	1
1.2	MOS SRAM cell and peripheral circuit operation	1
1.3	bipolar SRAM technologies, silicon on insulator (SOI) technology	1
1.4	silicon on insulator (SOI) technology, advanced SRAM architectures and technologies	1
1.5	application specific SRAMs	1

1.6	**(DRAMs)**: DRAM technology development, CMOS CRAMs	1
1.7	DRAMs cell theory and advanced cell structures- BiCMOS DRAMs	1
1.8	soft error failure in DRAMs, Advanced DRAM designs and architecture	1
1.9	application specific DRAMs.	1
	Module 2 : **Non volatile Memories**	
2.1	Masked Read only memories (ROMs): High density ROMs,	1
2.2	programmable read-only memories (PROMs)- bipolar PROMs, CMOS PROMs	2
2.3	erasable (UV)- Programmable read-only memories (EPROMs)- Floating Gate EPROM cell- one, time programmable (OTP) Eproms,	2
2.4	Electrically Erasable PROMs (EEPROMs), EEPROM technology and architecture, non-volatile SRAM	2
2.5	Flash memories (EPROMs or EEPROM), Advanced flash memory architecture.	2
	Module 3: **Memory fault modelling, testing and memory design for Testability and fault tolerance**	
3.1	RAM fault modelling	1
3.2	Electrical testing	1
3.3	Pseudo random testing	1
3.4	Megabit DRAM Testing Non Volatile Memory Modelling And Testing	2
3.5	IDDQ fault modelling and testing,	1
3.6	Application Specific Memory Testing.	1
	Module 4 : **Semiconductor memory reliability**	
4.1	General Reliability issues	1
4.2	RAM failure modes and mechanism	1
4.3	Non Volatile Memory Reliability	1

4.4	Reliability Modelling And Failure Rate Prediction	2
4.5	Design For Reliability, Reliability Test Structures, Reliability Screening And Qualification	2
	Module 5: **Advanced memory technologies and high-density memory packaging technologies:**	
5.1	Ferroelectric Random Access Memories (FRAMs)	1
5.2	Gallium Arsenide (GaAs) FRAMs	1
5.3	Analog memories ,magneto resistive random access memories (MRAMs)	2
5.4	Experimental memory devices	1
5.5	Memory hybrids and MCMs (2D), Memory stacks and MCMs (3D)	1
5.6	Memory MCM testing and reliability issues	1
5.7	memory cards- high density memory packaging future directions.	1

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS)
KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E203D**

Course Name: SEMICONDUCTOR MEMORIES

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

13. Draw and explain the SRAM cell Structure.
14. Draw the mask ROM development stages and explain..
15. What is bridging fault? .Explain with Supporting Data.
16. Briefly describe the main charge loss mechanisms in EPROM.
17. Differentiate the key differences between FRAMS and EEPROMs.

PART B

Answer any five questions. Each question carries 8 marks

6. Explain different types of application specific SRAMs.
7. Explain Advanced FLASH memory architectures with automatic Erase Algorithm.
8. Which are the most commonly used RAM Memory fault models? Expalin.
9. Explain General Semiconductor memory reliability issues.
10. Draw the FRAM cell structure and explain its operation.
11. Explain SRAM reliability issues.
12. Explain the soft error failures in DRAMs.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E203E	EMBEDDED SYSTEM DESIGN	PROGRAM ELECTIVE III	3	0	0	3	3

Preamble: The course, Embedded System Design, provides a substantial knowledge base in enabling the student to design complex embedded systems from scratch. Major topics covered in-depth are knowledge of various embedded system technologies with a stress on processor technologies, peripherals, and communication interfaces. The course also covers the aspects of hardware-software co-design and techniques for program modelling. The student will get oriented in concepts like Cache Memory, Pipeline Architecture, and in the design of Single Purpose Processors. This course facilitates the student with the knowledge of various components needed to design an embedded system meeting the requirement specification. The course also deals with case studies where different processor architectures are used to design embedded systems with an emphasis on the VLSI perspective. These case studies enable the student to do design selection and design comparisons based on various design optimization parameters and requirement specifications.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs. After the completion of the course, the student will be able to

CO 1	Understand and apply various aspects of hardware and software architectures in embedded system design.
CO 2	Differentiate various embedded system technologies and their implications on embedded system design.
CO 3	Design, analyse and optimise different single-purpose processor architectures.
CO 4	Evaluate and analyse different cache memory configurations. Distinguish various communication protocols and interfaces.
CO 5	Assess different embedded system case studies.
CO 6	Design an embedded system by identifying the best processor architecture based on the requirement specifications and design optimization matrices.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2	3			
CO 2	1	2				
CO 3	1	2	3	4		
CO 4	1		4			
CO 5	1	2	4			6
CO 6	1	2	3	4	5	6

Assessment Pattern

Course name	EMBEDDED SYSTEM DESIGN		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	**CIE marks**	**ESE marks**	**ESE Duration**
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Introduction to Embedded Systems: Introduction, common characteristics and categories of embedded systems, general requirements of embedded systems, design metrics and its optimization, embedded system development process, an overview of embedded system architecture, hardware architecture, software architecture, hardware-software co-design, computational models, introduction to unified modelling language, hardware-software trade-offs.

MODULE 2 (8 hours)

General-purpose Processors & Application Specific Instruction-Set Processors: Embedded System Technologies, General-purpose processors, pipeline, pipeline hazards, superscalar and VLIW architectures, Application Specific Instruction-Set Processors (ASIP's). Selecting a Microprocessor / General Purpose Processor.

MODULE 3 (8 hours)

Single Purpose Processors (Standard & Custom): Standard SPP: Timers, Counters, Watchdog Timer, Real-Time Clock, UART, Pulse Width Modulator, LCD Controller, Keypad Controller. **Custom SPP:** RT- level Custom Single purpose Processor Design, Optimizing the original program, Optimizing the FSMD, Optimizing the datapath, and optimizing the FSM.

MODULE 4 (8 hours)

Memory & Communication Protocols: Memory: Memory classification, ROM, RAM, Memory hierarchy, Cache, Cache Mapping, Cache write policy, Cache update policy, Cache Coherency. **Communication Protocols:** Serial - RS232, RS422/RS485, I2C, SPI, USB, Ethernet, CAN. Parallel - PCI bus, AMBA bus. Wireless - Bluetooth, IEEE 802.11, LoRaWAN.

MODULE 5 (8 hours)

Case Study – Digital Camera & Control System: Digital Camera: User's perspective, designer's perspective, specification, informal functional specification, non-functional specification, executable specification. Design, Implementation, and Comparison - microcontroller-based implementation, fixed point FDCT implementation, hardware FDCT implementation. **Control System:** Open-loop and closed-loop control systems, an open-looped automobile cruise controller, a closed-loop automobile cruise-controller, general

control systems and PID controllers, practical issues related to computer-based control, and benefits of computer-based control implementations.

Reference Books

1. Frank Vahid and Tony Givargis, Embedded System Design-A Unified Hardware/Software Introduction", John Wiley & Sons, 2002.
2. William Stallings, Computer Organization and Architecture : Designing for Performance, Pearson Education 2016
3. Marilyn Wolf, Computer as Components Principles of Embedded Computing System Design, Elsevier, 2012
4. Steve Heath, Butterworth Heinemann, "Embedded System Design." Newnes, 2nd edition (December 25, 2002)
5. Jorgen Staunstrup, Wayne Wolf (editors), Hardware/Software Co-Design: Principles and Practice, Springer, 1997
6. Gajski and Vahid, "Specification and Design of Embedded systems", Prentice Hall.
7. Rajkamal, "Embedded systems: Architecture, Programming and Design", TMH, 2012.
8. Shibu K.V.," Introduction to Embedded Systems, Tata McGraw Hill Education Private Limited, 2010.
9. Alexandru Forrai, Embedded Control System Design: A Model Based Approach, Springer, 2013
10. Alberto Sangiovanni-Vincentelli, Haibo Zeng • Marco Di Natale, Peter Marwedel, Embedded Systems Development : From Functional Models to Implementations, Springer, 2014
11. Bruce Powel Douglass, Real-Time UML Workshop for Embedded System, Elsevier; First edition (1 January 2010)
12. Kraig Mitzner, Complete PCB Design Using OrCAD Capture and PCB Editor, Elsevier Inc, 2009

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Introduction, Common Characteristics, and Categories of embedded systems.	1
1.2	General requirements of embedded systems – performance, size, reliability and ruggedness, cost-effectiveness, power consumption, user interfaces, software updating capability.	1
1.3	Design challenges, design metrics, and optimization .	1
1.4	Embedded System Development Process, Overview of Embedded System Architecture.	1
1.5	Hardware Architecture – CPU, memory, input devices, output devices, communication interfaces, application specific circuitry.	1
1.6	PCB concepts: PCB, Multilayer PCB, stack up, track, via, signal integrity basics (impedance, reflection, ringing, cross talk, simultaneous switching noise), component packages (through-hole and SMT), PCB assembly (manual vs automatic), and PCB testing.	1
1.7	Software Architecture, challenges, and issues related to embedded software development, fundamental issues in	1

	hardware software co-design,	
1.8	Computational models in Embedded Design, Introduction to Unified Modeling Language, hardware-software Trade-offs.	1
	Module 2	
2.1	Embedded System Technologies: Processor Technology, IC Technology, and Design Technology.	2
2.2	General-purpose Processors: Basic architecture, Datapath, Control unit	1
2.3	Pipelining, Standard 5 stage pipeline, Pipeline Hazards.	3
2.4	Superscalar and VLIW architectures.	1
2.5	Application Specific Instruction-Set Processors (ASIP's): Microcontrollers, DSP, Less- General ASIP environments. Selecting a Microprocessor / General Purpose Processor - performance parameters, Amdahl's law, and benchmark.	1
	Module 3	
3.1	Standard SPP: Timers, Counters, Watchdog Timer, Real-Time Clock.	1
3.2	Standard SPP: UART, Pulse Width Modulator, LCD Controller, Keypad Controller.	1
3.3	Custom SPP: RT- level Custom Single purpose Processor Design	5
3.4	Custom SPP: Optimizing the original program, optimizing the FSMD, optimizing the datapath, and optimizing the FSM.	1
	Module 4	
4.1	Memory: Memory classification, ROM, RAM, Memory hierarchy, Cache, Cache Mapping, Cache write policy, Cache update policy.	3
4.2	Serial: RS232, I2C (including arbitration), SPI, USB, Ethernet, CAN.	3
4.3	Parallel: PCI bus, AMBA bus.	1
4.4	Wireless: Bluetooth, IEEE 802.11, LoRaWAN	1
	Module 5	
5.1	Digital Camera: User's perspective, Designer's perspective, Specification, Informal Functional specification, Non-functional specification. Executable specification.	1
5.2	Digital Camera: Design, Implementation, and Comparison - microcontroller based implementation, fixed point FDCT implementation, hardware FDCT implementation.	3
5.3	Control System: Open-loop and closed loop control systems, an open- looped automobile cruise controller, a closed-loop automobile cruise- controller, and General control systems (P,PI, PD, and PID controllers).	3
5.4	Practical Issues Related to computer-based control, Benefits of computer-based control Implementations	1
	Total	40

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E203E**

Course Name: **EMBEDDED SYSTEM DESIGN**

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Write a short note on five common characteristics of Embedded Systems with examples.
2. What is pipelining? "Increasing the number of pipelines stages improves the processor performance" Justify the statement with example.
3. Briefly explain about RTC with a neat diagram. Explain about the power backup scheme implemented with RTC. Why 32.768 KHz is given as the standard frequency for RTC clock?
4. List down any two signal component of I2C bus. Briefly explain the I2C arbitration process with neat diagram.
5. In the context of digital camera what is informal functional specification and what is refined functional specification? Considering a digital camera discuss on the statement "a design metric can be both constrained and optimized".

PART B

Answer any five questions. Each question carries 8 marks.

6. Analyse the hardware architecture of an embedded system with a neat diagram.
7. What are Pipeline Hazards? Categorise various Pipeline Hazard and discuss on methods to solve them.
8. Develop an algorithm, draw the state diagram, and design the datapath of a custom single purpose processor to determine the sum of digits of a number. Propose the block diagram and FSMD of its controller.
9. a. A 64 bit microprocessor running at 100 MHz speed is designed with an L1 cache which interacts with a DRAM of 50 cycles read time. Four design suggestions are listed below. Calculate the Average Memory Access Time, identify the best design and analyze the same.

i. L1 cache,1K size, miss rate = 20%, hit time = 3 cycles
ii. L1 cache,2K size, miss rate = 15%, hit time = 4 cycles
iii. L1 cache,4K size, miss rate = 10%, hit time = 5 cycles

b. Consider a cache with 4 memory locations with LRU replacement policy. Memory blocks 5, 3, 20, 45, 3, 5, 4, 20, 4, 45, 23 are requested by processor. What will be the status of cache after this operation?

10. Analyse the closed loop cruise control system with a neat diagram and compare the Proportional controller with Proportional Integral controller.
11. Develop an algorithm, draw the state diagram, and design the datapath of a custom single purpose processor to implement pow (x, n) function. Propose the block diagram and FSMD of its controller.
12. a. Consider a system with 3 level caches. Access times of Level 1 cache, Level 2 cache, Level 3 cache and main memory are 1 ns, 15ns, 30ns, and 500 ns, respectively. The hit rates of L1, L2 and L3 caches are 0.85, 0.92 and 0.95, respectively. What is the average access time of the system neglecting the miss penalties?

b. The floating point operations of a processor need to be enhanced by introducing a new advanced FPU unit. Let the new FPU is 10 times faster on floating point computations than the original processor. Assuming a program has 40% floating point operations, what is the overall speedup gained by incorporating the enhancement?

SEMESTER II
PROGRAM ELECTIVE IV

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E204A	LOW POWER VLSI	PROGRAMME ELECTIVE IV	3	0	0	3	3

Preamble: This course aims to develop students a good knowledge on designing low power VLSI circuits by estimating and analysing power dissipation using different methodologies and there-by implementing low power design methodologies in different levels of design.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design chips for battery powered systems and high-performance circuits not exceeding power limits and examine analyze power dissipation using simulation.
CO 2	Examine the power dissipation using power analysis like probabilistic techniques and to understand power dissipation in clock distribution for accurate working of circuit.
CO 3	Design low power circuits at circuit and logic level.
CO 4	Analyze performance management techniques and low power memory design techniques.
CO 5	Understand advanced topics like adiabatic switching.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2	3	4		
CO 2	1	2	4			
CO 3	1	2	3	4		
CO 4	1	2	4			
CO 5	1	2				

Assessment Pattern

Course name	LOW POWER VLSI .		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10

Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (9 hours)

Need for low power VLSI chips and Simulation Power analysis: Introduction - Need for low power VLSI, charging and discharging capacitance, short circuit current in CMOS circuit, CMOS leakage current, static current, Basic principles of low power design, Simulation Power analysis: SPICE circuit simulation, Gate level logic simulation - capacitive power estimation, static state power, gate level capacitance estimation.

MODULE 2 (8 hours)

Probabilistic Power analysis and Low power Clock Distribution: Probabilistic power analysis: Random logic signals, Probability & frequency, Probabilistic power analysis techniques, Low power Clock Distribution: Power Dissipation In Clock Distribution, Single Driver Vs Distributed Buffers.

MODULE 3 (8 hours)

Low Power Design- Circuit and Logic level: Circuit level: Transistor & Gate sizing, Network restructuring & reorganization, Special Latches & flip-flops, Logic level: Gate Reorganization, Signal Gating, Logic Encoding.

MODULE 4 (8 hours)

Low power Architecture & Systems: Power & Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Low Power Memory Design: Low power static RAM – organization of static RAM, MOS static RAM cell, Banked organization of SRAMs.

MODULE 5 (8 hours)

Adiabatic switching: Adiabatic switching, Adiabatic charging, Adiabatic amplification, one stage and twostage adiabatic buffer in conventional system, fully adiabatic sequential circuits, stepwise charging, pulsed power supplies.

Reference Books

1. Rabaey, Pedram, “Low power design methodologies” Springer Science & Business Media, 2012.
2. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002.
3. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000.
4. Anatha P Chandrakasan, Robert W Brodersen, "Low power digital CMOS Design", Kluwer Academic.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1 **Need for low power VLSI chips and Simulation Power analysis**	**9 hours**
1.1	Introduction - Need for low power VLSI chips	1
1.2	Charging and Discharging capacitance	1
1.3	Short Circuit current in CMOS circuit	1
1.4	CMOS leakage current, Static current	1
1.5	Basic principles of low power design	1
1.6	**Simulation Power analysis:**	1
1.6.1	SPICE circuit simulation	1
1.6.2	**Gate level logic simulation** - Capacitive power estimation, Static state power, Gate level capacitance estimation	2
	Module 2 **Probabilistic Power analysis and Low power Clock Distribution**	**8 hours**
	Probabilistic power analysis:	

2.1	Random logic signals	1
2.2	Probability & frequency	1
2.3	Probabilistic power analysis techniques	3
	Low power Clock Distribution:	
2.4	Power Dissipation In Clock Distribution	1
2.5	Single Driver Vs Distributed Buffers	2
	Module 3 **Low Power Design- Circuit and Logic level** **hours**	**8**
	Circuit level:	
3.1	Transistor & Gate sizing	2
3.2	Network restructuring & reorganization	1
3.3	Special Latches & flip-flops	2
	Logic level	
3.4	Gate Reorganization	1
3.5	Signal Gating	1
3.6	Logic Encoding	1
	Module 4 **Low power Architecture & Systems** **hours**	**8**
4.1	Power & Performance Management	1
4.2	Switching Activity Reduction	2
4.3	Parallel Architecture With Voltage Reduction	2
4.4	**Low Power Memory Design**	
4.4.1	Low power static RAM – Organization of static RAM	1
4.4.2	MOS static RAM cell, Banked organization of SRAMs	2
	Module 5 **Adiabatic switching** **hours**	**8**
5.1	Adiabatic switching – Adiabatic charging	2
5.2	Adiabatic amplification	1
5.3	One stage and Two stage adiabatic buffer in conventional system	2
5.4	Fully Adiabatic Sequential Circuits	1
5.5	Stepwise Charging	1
5.6	Pulsed Power Supplies	1

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E204A**

Course Name: LOW POWER VLSI

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Illustrate short circuit current variation in CMOS circuits with load capacitance and input signal slope.
2. Explain different types of clock driving scheme.
3. Illustrate how the network restructuring helps in leakage power reduction.
4. Discuss the concepts and operation of 6T SRAM memory cell with all necessary diagrams and tables.
5. Discuss fully adiabatic system and formulate E_{total}.

PART B

Answer any five questions. Each question carries 8 marks.

6. Using Gate level Capacitance estimation, analyze the gate level power dissipation of a circuit.
7. Discuss about charging and discharging capacitance of CMOS device. Derive an expression for power dissipation.
8. Derive an expression for total transition density and explain gate level power analysis using transition density.
9. Using necessary mathematical equations, explain how you will relate the static probability of a digital signal to switching frequency.
10. Illustrate how the transistor sizing helps in leakage power reduction.
11. Explain how switching activities can be reduced in CMOS digital systems.
12. Explain adiabatic amplification with a neat diagram. Derive an expression for $E_{load.}$

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E204B	VLSI SYSTEM TESTING	PROGRAMME ELECTIVE IV	3	0	0	3	3

Preamble: This course aims to provide a strong base in digital VLSI Testing. In this course, different fault models and methods for test generation and application are discussed. Syllabus covers concepts of Scan architecture and BIST. The course equips the learner to design a test environment.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Interpret fault models and to create collapsed fault list.
CO 2	Develop simulators and to calculate SCOAP measures.
CO 3	Generate test vectors for combinational and sequential circuits.
CO 4	Generate test vectors for memory faults and delay faults.
CO 5	Design scan architecture and pattern generators.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2	4			
CO 2	1	2	3	4		
CO 3	1	2	3	4		
CO 4	1	2	3	4		
CO 5	1	2	3		5	

Assessment Pattern

Course name	VLSI SYSTEM TESTING		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	**Test 1 (% Marks)**
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Fault Models and Fault Collapsing: Role of Testing, Structural Testing, Fault Modeling, Glossary of Fault Models, Fault Equivalence, Fault Collapsing, Fault Dominance, Check Point Theorem.

MODULE 2 (8 hours)

Simulation and Testability Measures: True Value Simulator, False Simulator, Algorithms for True Value Simulation – Compiled Code Simulation, Event Driven Simulation, Algorithms for Fault Simulation – Serial Fault Simulation, Parallel Fault Simulation, Combinational SCOAP Measures, Sequential SCOAP Measures.

MODULE 3 (7 hours)

Circuit Test Generation: ATPG Algebras – Roth's 5 Valued Algebra, Muth's 9 Valued Algebra, Algorithm

Types, Redundancy Identification, Combinational ATPG Algorithms – D-Algorithm, PODEM, Sequential ATPG Algorithm – Time Frame Expansion Method.

MODULE 4 (9 hours)

Memory Test and Delay Test: Memory Faults, Fault Manifestations, Failure Mechanisms, March Test Notations, Fault Modeling, Reduced Functional Faults, Relation between Fault Models and Physical Defects, Delay Test Problem, Test Generation for Combinational Circuits, Transition Faults, Delay Test Methodologies.

MODULE 5 (7 hours)

DFT and BIST: Ad-Hoc DFT Methods, Scan Design Rules, Tests for Scan Circuits, Overheads of Scan Design, Partial-Scan Design, Variations of Scan, Random Logic BIST – BIST Process, BIST Implementations, Pseudo Random Pattern Generation using Standard LFSR, using Modular LFSR, BIST Response Compaction using LFSR, Multiple Input Signature Register.

Reference Books

1. Viswani D Agarwal and Michael L Bushnell, "Essentials of Electronic Testing of Digital Memory and Mixed Signal VLSI Circuits", Springer, 2000.
2. M. Abramovici, M A Breuer and A D Friedman, "Digital systems Testing and Testable Design", IEEE Press, 1994.
3. Niraj Jha and Sanjeep K Gupta, "Testing of Digital Systems", Cambridge University Press, 2003.
4. L-T Wang, C-W Wu, and X. Wen "VLSI Test Principles and Architectures: Design for Testability", Academic Press, 2006.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1 **Fault Models and Fault Collapsing** **8 hours**	
1.1	Role of Testing	1
1.2	Structural Testing, Fault Modeling, Glossary of Fault Models	3
1.3	Fault Equivalence, Fault Collapsing, Fault Dominance, Check Point Theorem	4
	Module 2 **Simulation and Testability Measures** **8 hours**	
2.1	True Value Simulator, False Simulator, Algorithms for True Value Simulation – Compiled Code Simulation, Event Driven Simulation, Algorithms for Fault Simulation – Serial Fault Simulation, Parallel Fault Simulation	4
2.2	Combinational SCOAP Measures, Sequential SCOAP Measures	4
	Module 3 **Circuit Test Generation** **7 hours**	

3.1	ATPG Algebras – Roth's 5 Valued Algebra, Muth's 9 Valued Algebra, Algorithm Types, Redundancy Identification	2
3.2	Combinational ATPG Algorithms – D-Algorithm, PODEM	3
3.3	Sequential ATPG Algorithm – Time Frame Expansion Method	2
	Module 4 **Memory Test and Delay Test** **9 hours**	
4.1	Memory Faults, Fault Manifestations, Failure Mechanisms	1
4.2	March Test Notations, Fault Modeling, Reduced Functional Faults, Relation between Fault Models and Physical Defects	4
4.3	Delay Test Problem, Test Generation for Combinational Circuits, Transition Faults, Delay Test Methodologies	4
	Module 5 **DFT and BIST** **7 hours**	
5.1	Ad-Hoc DFT Methods, Scan Design Rules, Tests for Scan Circuits, Overheads of Scan Design	2
5.2	Partial-Scan Design, Variations of Scan	1
5.3	Random Logic BIST – BIST Process, BIST Implementations, Pseudo Random Pattern Generation using Standard LFSR, using Modular LFSR	2
5.4	BIST Response Compaction using LFSR, Multiple Input Signature Register	2

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

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MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E204B**

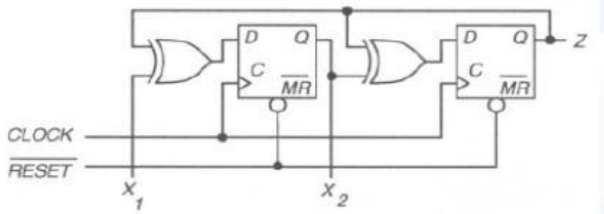
Course Name: VLSI System Testing

Max. Marks:60 Duration: 3 hours

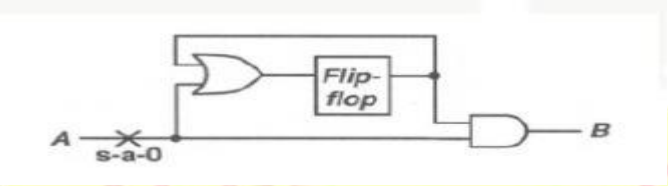
PART A

Answer all questions. Each question carries 4 marks.

1. What is the significance of fault equivalence set? Illustrate with an example.
2. Calculate the sequential SCOAP testability measures for the circuit shown below. Assume synchronous clock.



3. Derive a test for this fault using nine valued logic.

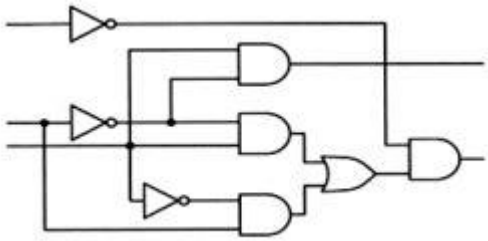


4. What are the robust path delay sensitization conditions for NAND gate and OR gate?
5. For a circuit with 1,00,000 gates and 2,000 flipflops, connected in a single scan chain, what is the gate overhead?

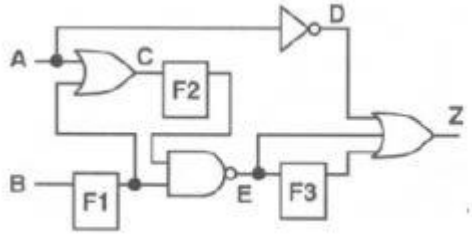
PART B

Answer any five questions. Each question carries 8 marks.

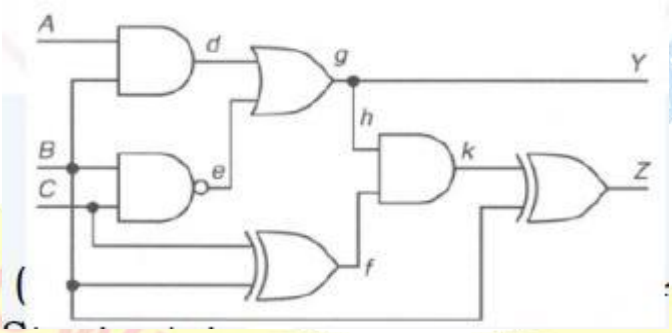
6. a. What is Check Point Theorem?
   b. Identify the check points of the following circuit.



7. Calculate the combinational SCOAP values for the circuit shown in 6(b).
8. Derive a test pattern to detect D Stuck-at-0.



9. Consider the circuit shown below. Use D-Algorithm to derive a test vector for h Stuck-at-0.



10. Does MATS algorithm (w0); (r0, w1); (r1) detect Stuck-at faults? Justify for cases, Stuck-at-0 and Stuck-at-1.
11. For the characteristic equation x3 + x2 + x + 1,
    a. draw standard LFSR
    b. derive companion matrix Ts for the standard LFS
12. With relevant block diagrams and waveforms, explain Enhanced-Scan Test.
13.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E204C	HIGH SPEED DIGITAL SYSTEM DESIGN	PROGRAMME ELECTIVE IV	3	0	0	3	3

Preamble :

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits
- To introduce the architectures of programmable devices.
- To introduce design and implementation of digital circuits using programming tools.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Adapt to go far into the world of high speed digital design.
CO 2	Describe the wire model inventory, noise, signaling, and synchronization ideas related to high-speed design.
CO 3	Understanding the trade-offs between noise immunity, power, speed, and other factors can help you build high-speed systems and other linked domains
CO 4	To learn troubleshooting clock problems in VLSI designs

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1				5	
CO 2	1	2				
CO 3	1	2		4		
CO 4	1	2	3	4		

Assessment Pattern

Course name	HIGH SPEED DIGITAL SYSTEM DESIGN		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 8 marks. Total duration of the examination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Frequency, time and distance, Knee Frequency and its significance, Propagation Delay, Capacitance and Inductance Effects, High speed properties of logical gates, Speed and power. Geometry and Electrical properties of wires, Electrical model of wires, Lattice Diagram Analysis of Transmission Lines, Simple and Special Transmission Lines.

MODULE 2 (6 hours)

Power supply network, Local power regulation, IR drops, Area bonding, On chip bypass capacitors, Bypass Capacitor Design, Symbiotic bypass capacitors, Power supply isolation

MODULE 3 (7 hours)

Power supply Noise, Cross talk, Noise, budgeting and SNR, Signal Interference, inter-symbol Interference, Noise sources in digital system, Statistical Analysis.

MODULE 4 (10 hours)

Signalling modes for transmission lines, signalling over lumped transmission media, signalling over RC interconnects, driving lossy LC lines, simultaneous bi-directional Signalling, Terminator circuits. PLL and DLL based clock aligners.

MODULE 5 (8 hours)

Timing fundamentals, Timing properties of clocked storage elements, signals and events, Open loop Timing, level sensitive clocking, Pipeline Timing, Closed loop Timing, Synchronisation failure and metastability, probability of synchronization failure Hierarchy of synchronizer design – delay line, 2-register and FIFO mesochronous synchronizers.

Text Books

1. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbook of Black Magic by",3rd Edition, (Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library), 2006
2. Stephen H. Hall, Garrett W. Hall, and James A. McCall " High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices" by , Wiley , 2007
3. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen "High Speed CMOS Design Styles", Springer Wiley 2006
4. Ramesh Harjani "Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems)" World Scientific Publishing Company 2006

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Frequency, time and distance, Knee Frequency and its significance, Propagation Delay, Capacitance and Inductance Effects	3
1.2	High speed properties of logical gates, Speed and power. Geometry and Electrical properties of wires, Electrical model of wires.	3
1.3	Lattice Diagram Analysis of Transmission Lines, Simple and Special Transmission Lines.	2
	Module 2	
2.1	Power supply network, Local power regulation, IR drops, Area bonding,	2
2.2	On chip bypass capacitors, Bypass Capacitor Design	2
2.3	Symbiotic bypass capacitors	1
2.4	Power supply isolation	1
	Module 3	
3.1	Power supply Noise	2
3.2	Cross talk, Noise budgeting and SNR	2
3.3	Signal Interference, inter-symbol Interference	2
3.4	Noise sources in digital system , Statistical Analysis	1
	Module 4	

4.1	Signalling modes for transmission lines	2
4.2	signalling over lumped transmission media	2
4.3	signalling over RC interconnects, driving lossy LC lines	2
4.4	simultaneous bi-directional Signalling	2
4.5	Terminator circuits. PLL and DLL based clock aligners.	2
	Module 5	
5.1	Timing fundamentals, Timing properties of clocked storage elements,.	1
5.2	signals and events, Open loop Timing, level sensitive clocking	1
5.3	Pipeline Timing, Closed loop Timing.	1
5.4	Synchronisation failure and metastability,	2
5.5	probability of synchronization failure Hierarchy of synchronizer design – delay line	2
5.6	2-register and FIFO mesochronous synchronizers	1

Model Question Paper

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MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E204A**

Course Name: HIGH SPEED DIGITAL SYSTEM DESIGN

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. Describe the electrical properties of wires.
2. Differentiate bipolar versus unipolar signalling. Draw the clocked RZ and clocked NRZ wave forms for the data 101100.
3. Discuss the effect of cross talk in power supply network.
4. Write about simultaneous signaling.
5. Discuss the importance of set up time and hold time with help of neat diagrams.

PART B

Answer any five questions. Each question carries 8 marks.

6. Discuss the importance of knee frequency in the performance of high-speed digital circuits
7. A 20m-longless transmission line with Zo=75Ω operating at 1 MHz is terminated with a load ZL=100+j150Ω, find

a. The reflection coefficient

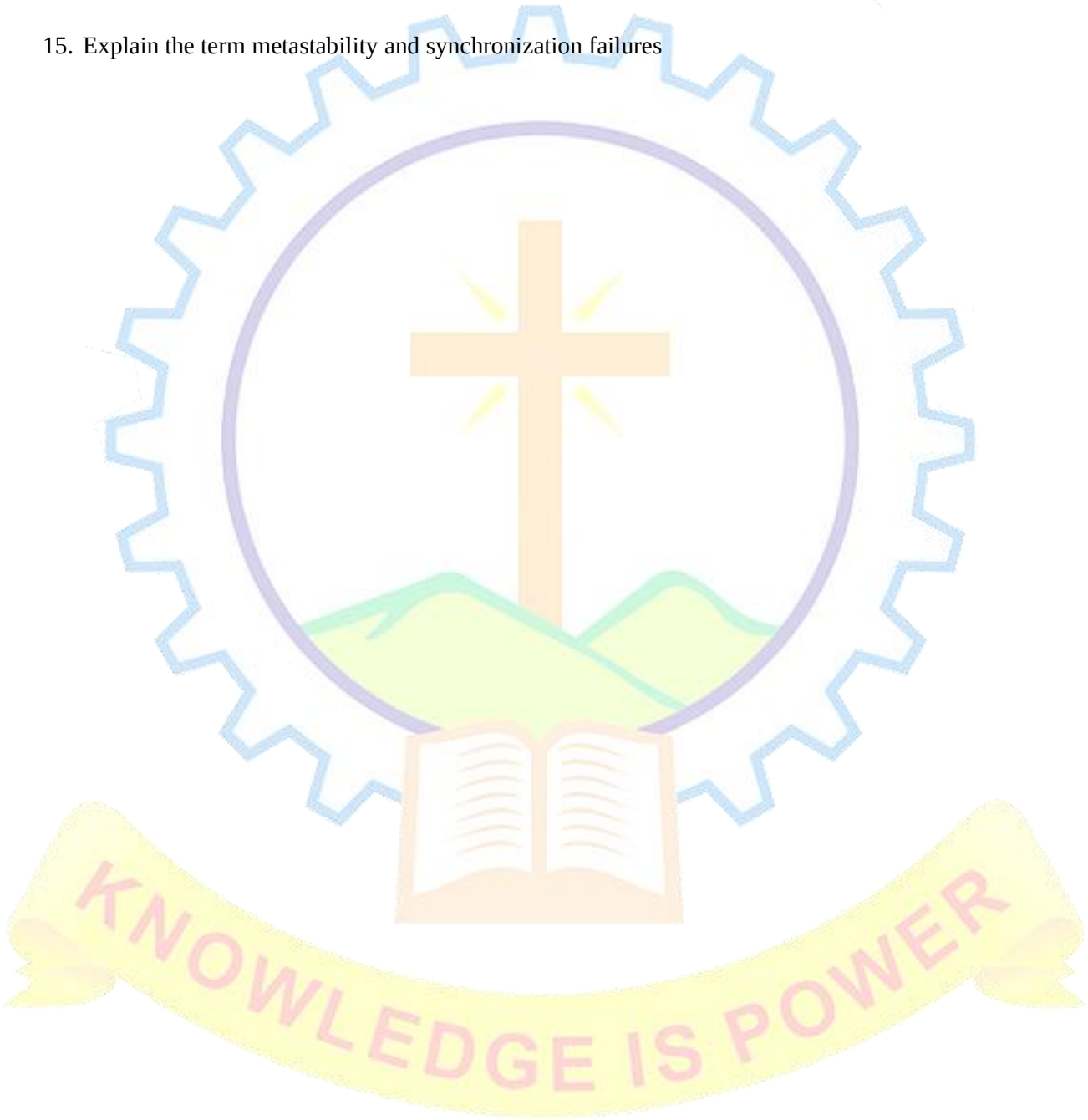
b. The standing wave ratio S

8. write a short note on area bonding, IR dropping, on chip bypass capacitors
9. Discuss the different types of power supply isolation techniques.

10. a. Discuss the noise sources in digital system

    b. discuss the importance of noise budgeting and inter symbol interference terms in ciruit design
11. Explain in detail different power supply noises.

12. Explain in detail signalling over lumped transmission line
13. Explain simultaneous and bidirectional signaling
14. List the different on chip clock distribution networks? Explain any one of them with relevant diagrams.
15. Explain the term metastability and synchronization failures



CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E204D	DEEP LEARNING	PROGRAM ELECTIVE IV	3	0	0	3	3

Preamble: This course provides an introduction to key concept in deep learning and equip students with knowledge required to develop best deep learning solutions for real world problems in domains such as computer vision, natural language processing etc.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs. After the completion of the course the student will be able to

CO 1	Demonstrate the uses and limitations of fully connected neural networks
CO 2	Compare different CNN networks for classification and detection in terms of architecture, performance and computational requirements
CO 3	Develop a convolutional neural network for a real-world application
CO 4	Apply regularization and optimization techniques in CNN training
CO 5	Demonstrate the use of RNNS and LSTM for analysing sequential data
CO 6	Apply the concepts of attention models, transformers and generative models

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3					
CO 2	3					
CO 3	3		3	3	3	
CO 4	3					
CO 5	3					
CO 6	3		3	3		

Assessment Pattern

Course name	EMBEDDED OPERATING SYSTEM		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application,analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of whichstudent shall answer any five. Each question can carry 8 marks. Total duration of theexamination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours): Introduction to Machine Learning

Introduction: Supervised Vs. Unsupervised Learning, Classification Vs. Regression, Machine Learning Vs. Deep Learning
Machine Learning System Design: Data-driven Approach, Datasets: Training, Testing and Validation Sets, Over fitting and Under fitting, Hyper parameters,
K-nearestneighbour classification
Linear classification: Loss function, Multiclass SVM,Softmax classifier. Optimization, Numeric andAnalytic gradients.

MODULE 2 (7 hours): Neural Networks

Deep feedforward networks/ Multilayer perception: Perceptron, activation functions, Example: Learning XOR, Architecture of deep neural network
Back propagation, Gradient-Based Learning.

Convolutional Neural Networks: Convolution, Pooling Layers, spatial arrangement, layer patterns, layer sizing patterns.

MODULE 3 (6 hours): Training Neural Networks

Initialization, batch normalization, Hyper parameter optimization.
Optimization algorithms: SGD, Momentum, Adagrad, RMS Prop, Adam
Regularization methods: L1 and L2 regularization, Early stopping, drop outs, ensembles, data augmentation, Update rules, transfer learning.

MODULE 4 (9 hours): CNN architectures

AlexNet, VGG Net, ResNet, Inception Net
Object Detection: RCNN, Fast RCNN, Faster RCNN, YOLO, Mask RCNN
Recurrent Neural Networks: RNN, Bidirectional RNN, LSTM, GRU

MODULE 5 (10 hours): Attention Models, Transformers and Generative Models

Attention: Multimodal attention, Self-Attention
Transformers: BERT and vision transformer
Autoencoders, Variational auto encoders, Generative Adversarial Network

Text Books

1. Ian Goodfellow, YoshuaBengio, and Aaron Courville. Deep learning. MIT press,2016.
2. Francois Chollet. Deep learning with Python. Simon and Schuster, 2021.
3. Ivan Vasilev. Advanced Deep Learning with Python: Design and implement advanced next-generation AI solutions using TensorFlow and PyTorch. Packt Publishing Ltd, 2019.
4. C. M. Bishop, Pattern Recognition and Machine Learning, Springer, 2006
5. Michael A Nielsen. Neural networks and deep learning. Determination press, 2015.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1: Introduction to Machine Learning	
1.1	Introduction: Supervised Vs. Unsupervised Learning, Classification Vs. Regression, Machine Learning Vs. Deep Learning	1
1.2	Machine Learning System Design: Data-driven Approach, Datasets: Training, Testing and Validation Sets, Over fitting and Under fitting, Hyper parameters, K-nearestneighbour classification	3
1.3	Linear classification: Loss function, Multiclass SVM, Softmax classifier. Optimization, Numeric andAnalytic gradients.	4
	Module 2: Neural Networks	
2.1	Deep feedforward networks/ Multilayer perception: Perceptron, activation functions, Example: Learning XOR, Architecture of deep neural network	2

2.2	Back propagation, Gradient-Based Learning.	2
2.3	Convolutional Neural Networks: Convolution, Pooling Layers, spatialarrangement, layer patterns, layer sizing patterns.	3
	Module 3: Training Neural Networks	
3.1	Initialization, batch normalization, Hyper parameter optimization.	2
3.2	Optimization algorithms: SGD, Momentum, Adagrad, RMS Prop, Adam	2
3.3	Regularization methods: L1 and L2 regularization, Early stopping, drop outs, ensembles, data augmentation, Update rules, transfer learning	2
	Module 4: CNN architectures	
4.1	AlexNet, VGG Net, ResNet, Inception Net	3
4.2	Object Detection: RCNN, Fast RCNN, Faster RCNN, YOLO, Mask RCNN	3
4.3	Recurrent Neural Networks: RNN, Bidirectional RNN, LSTM, GRU	3
	Module 5: Attention Models, Transformers and Generative Models	
5.1	Attention: Multimodal attention, Self-Attention	3
5.2	Transformers: BERT and vision transformer	3
5.3	Autoencoders, Variational auto encoders, Generative Adversarial Network	4
	Total	40

Model Question Paper

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Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E204D**

Course Name: DEEP LEARNING

Max. Marks:60 Duration: 3 hours

PART A

Answer all questions. Each question carries 4 marks.

1. There is huge gap between training accuracy and testing accuracy, while training a particular machine learning model. What might be the reason. Suggest possible methods of overcoming it

2. Draw the block diagram of a naïve inception block. What is the disadvantage of this block? Explain how adding 1x1 convolution helps to overcome the difficulty.

3. Consider a Convolutional Neural Network having three different convolutional layers in its architecture as

Layer-1	Filter Size – 3×3, Number of Filters – 10, Stride – 1, Padding – 0
Layer-2	Filter Size – 5×5, Number of Filters – 20, Stride – 2, Padding – 0
Layer-3	Filter Size – 5×5 , Number of Filters – 40, Stride – 2, Padding – 0

If we give a 51×51 RGB image as input to the network, then determine the dimension of the vector after passing through layer 3 in the architecture.

4. You have a dataset D1 with 1 million labelled training examples for classification, and dataset D2 with 100 labelled training examples. Your friend trains a model from scratch on dataset D2. You decide to train on D1, and then apply transfer learning to train on D2. State one problem your friend is likely to find with his approach. How does your approach address this problem?

5. Differentiate between soft attention and hard attention.

PART B

Answer any five questions. Each question carries 8 marks.

6. Astronomers are using a linear classifier to classify long exposed CCD images into star, nebula and galaxy. The predicted scores of this linear classifier, during one particular iteration of training is given below

Class	Test Image		
	Star	Nebula	Galaxy
Star	3.2	1.3	2.2
Nebula	5.1	4.9	2.5
Galaxy	-1.7	2	-3.1

Calculate the softmax loss for Nebula. Find minimum and maximum softmax loss, if there are C classes.

7. Draw the computational graph and calculate the analytical gradients at each node for the following function

$$f(w,x) = \frac{1}{1+e^{-(w_0x_0+w_1x_1+w_2)}}$$

where $ww_0 = 2$, $ww_1 = -3$, $ww_2 = -3$, $xx_0 = -1$, $xx_1 = -2$

8. Consider a CNN implemented with following arrangement.

Input 128x128x3
Conv 4- 10, stride 2, pad 0
Conv 9-10,stride 2, pad 2
Pool 2 stride 2, pad 0
Conv 3-5 stride 2, pad 0
FC 5

FC-N denotes fully connected layer with N neuron outputs. Conv M-N indicates convolution layer of size MxMxD, with M filters and D activation volume of previous layer. Pool 2 indicates 2x2 maxpooling layer. Find activation volume and number of parameters at each layer.

9. Write disadvantages of SGD. Explain how ADAM overcome it.

10. Imagine you were asked to write a poem in the writing style of John Keats. What kind of network will you use? Draw and explain the structure of identified network with equations.

11. You were asked to design an object detection frame work to be used in Google's autonomous car Waymo. The designed framework should be able to detect and identify multiple objects (pedestrians, other vehicles etc.) from images obtained from the camera feed of Waymo. Draw and explain the general structure of the network. Justify your answer.

12. Design a network to generate your photo in the style of Leonardo DaVinci'sMonalisa.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1E204E	STATIC TIMING ANALYSIS	PROGRAMME ELECTIVE IV	3	0	0	3	3

Preamble:

1. To understand the concepts of Static Timing Analysis in Industry standard digital design flow.
2. To study the concept design constraints in ASIC/FPGA designing.
3. To familiarize the various Timing Analysis Concepts and requirements in practical design flow.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs. After the completion of the course the student will be able to.

CO 1	Analyse the STA characteristics of a digital circuit and express the results
CO 2	Evaluate the Standard Cell Library model characteristics
CO 3	Analyse the interconnect parasitics of the circuit and calculate the delay
CO 4	Evaluate the Crosstalk and Noise of circuits based on models.
CO 5	Verify the timing based on the models and calculate the slack

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2	5			
CO 2	1	2		4		
CO 3	1	3				
CO 4	1	4				
CO 5	1	5				

Assessment Pattern

Course name	VLSI STRUCTURE FOR DSP		
Bloom's Category	**Continuous Internal Evaluation**		**End Semester Examination (% Marks)**
	Test 1 (% Marks)	**Test 2 (%Marks)**	
Remember	XX	XX	XX
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create	XX	XX	XX

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	40	60	3 Hours

Continuous Internal Evaluation Pattern:

Seminar* : 10 marks

Course based task/Micro Project//Data collection and interpretation/Case study : 10 marks

Test paper 1 (Module 1 and Module 2) : 10 marks

Test paper 2 (Module 3 and Module 4) : 10 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course

End Semester Examination Pattern: The end semester examination will be conducted by the college. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application,analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 4 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of whichstudent shall answer any five. Each question can carry 8 marks. Total duration of theexamination will be 3 Hrs.

SYLLABUS

MODULE 1 (8 hours)

Review of Pipelining and parallel processing for FIR filters, algorithmic strength reduction-introduction, parallel FIR filters, Discrete Cosine Transform and inverse DCT

MODULE 2 (8 hours)

Implementation of DCT and inverse DCT based on algorithm-architecture transformations.
Parallel architectures for Rank Order filters - Odd Even Merge sort architecture-Rank Order filter architecture-Parallel Rank Order filters-Running Order Merge Order Sorter-Low power Rank Order filter.

MODULE 3 (8 hours)

Pipelined and parallel recursive filters, Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined

pipelining and parallel processing of IIR filters.

MODULE 4 (8 hours)

Fast convolution: Introduction, Cook-Toom Algorithm, Modified Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution, cyclic convolution.

MODULE 5 (8 hours)

Scaling and round off noise - Round off noise in pipelined IIR filters – round off noise in lattice filters, pipelining of lattice IIR digital filters – low power CMOS lattice IIR filters

Text Books

1. J.Bhasker, Rakesh Chadha, "Static Timing Analysis for Nanometer Designs, A practical approach", Springer publications.
2. .Gangadharan, Sridhar, Churiwala, Sanjay "Constraining Designs for Synthesis and Timing Analysis": A Practical Guide to Synopsys Design Constraints (SDC), Springer publications.
3. Churiwala, Sanjay, Garg, Sapan "Principles of VLSI RTL Design" A Practical Guide, Springer publications.
4. Maheshwari, Naresh, Sapatnekar, S. "Timing Analysis and Optimization of Sequential Circuits" Springer publications.
5. HimanshuBhatnagar "Advanced ASIC Chip Synthesis" Using Synopsys Design Compiler Physical Compiler and PrimeTime, Springer publications.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
1	**Introduction Basics**; Crosstalk and Noise, Design Flow ; CMOS, FPGA & Asynchronous Designs, STA at Different Phases; Limitations; Power& Reliability Considerations . STA Concepts: CMOS Logic; Modeling of CMOS Cells; Switching Waveform; Propagation Delay; Slew of a Waveform;Skew between Signals; Timing Arcs and Unateness; Min and Max Timing Paths; Clock Domains; Operating Conditions	8
2	**Standard Cell Library Pin Capacitance**; Timing Modeling; Timing Models - Combinational Cells; Timing Models - Sequential Cells; State-Dependent Models; Interface Timing Model for a Black Box; Advanced Timing Modeling; Power Dissipation Modeling; Other Attributes in Cell Library; Characterization and Operating Conditions.	8
3.1	**Interconnect Parasitics:** RLC for Interconnect; Wireload Models; Representation of Extracted Parasitics; Representing Coupling Capacitances; Hierarchical Methodology; Reducing Parasitics for Critical Nets Delay Calculation: Overview; Cell Delay using Effective Capacitance; Interconnect Delay; Slew	8

	Merging; Different Slew Thresholds; Different Voltage Domains; Path Delay Calculation; Slack Calculation.	
4.1	**Crosstalk and Noise Overview**; Crosstalk Glitch Analysis; Crosstalk Delay Analysis; Timing Verification Using Crosstalk Delay; Computational Complexity; Noise Avoidance Techniques **Configuring the STA Environment:** Specifying Clocks; Generated Clocks; Constraining Input Paths; Constraining Output Paths; Timing Path Groups; Modeling of External Attributes; Design Rule Checks; Virtual Clocks; Refining the Timing Analysis; Point-to-Point Specification; Path Segmentation	8
5	**Timing Verification:** Setup Timing Check; Hold Timing Check; Multicycle Paths; False Paths; Half-Cycle Paths; Removal Timing Check; Recovery Timing Check; Timing across Clock Domains; Examples; Multiple Clocks **Interface Analysis:** IO Interfaces; SRAM Interface **Robust Verification:** On-Chip Variations; Time Borrowing; Data to Data Checks; Non-Sequential Checks; Clock Gating Checks; Power Management; Backannotation; Sign-off Methodology	8

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2024

Course Code: **M24EC1E204E**

Course Name: Static Timing Analysis

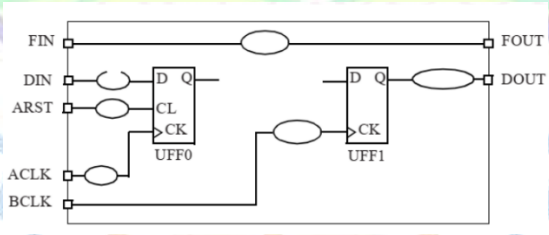
Max. Marks:60 Duration: 3 hours

PART A

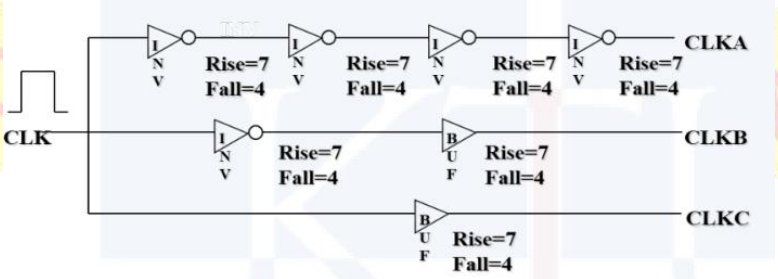
Answer all questions. Each question carries 4 marks.

1. Analyse the STA at Different Design Phases of an ASIC with a neat diagram based on the input?

2. Evaluate the Interface timing model for a Black Box given in Fig.1.What are the various timing arcs in the Black Box.



3. Analyse the clock circuit for Clock latency with reference Fig 2.



4. Apply the State-Dependent Model for XOR gate? Explain the different parameters in the Timing model?

5. Evaluate the CMOS cell characteristic and derive the electrically equivalent model specifying the capacitances in the nodes if nets are also considered?

PART B

Answer any five questions. Each question carries 8 marks.

6. With respect to the Table given in Fig.3 analyse the various terminologies related to the NLDM(Non Linear Delay model). Based upon the delay tables, calculate the rise delay of the inverter corresponding to an input fall transition of 0.3ns and an output load of 0.16pf.

```
pin (OUT) {
  max_transition : 1.0;
  timing() {
    related_pin : "INP1";
    timing_sense : negative_unate;
    cell_rise(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values (  /*  0.16      0.35     1.43 */ \
        /* 0.1 */   "0.0513,  0.1537,  0.5280", \
        /* 0.3 */   "0.1018,  0.2327,  0.6476", \
        /* 0.7 */   "0.1334,  0.2973,  0.7252");
      }
    cell_fall(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values (  /*  0.16      0.35      1.43 */ \
        /* 0.1 */   "0.0617,  0.1537,   0.5280", \
        /* 0.3 */   "0.0918,  0.2027,   0.5676", \
        /* 0.7 */   "0.1034,  0.2273,   0.6452");
    }
```

7. Evaluate the calculation of Cell Delays using Effective Capacitance method?
8. Evaluate the Crosstalk glitch analysis method with a diagram? What are the different types of glitches in Crosstalk glitch analysis?
9. Apply the Elmore's delay method for calculation of Interconnect Delays?
10. Evaluate the DC and AC thresholds in Crosstalk Glitch calculation?
11. Analyse what happens when a cell with one set of slew thresholds drives other cells with different set of slew threshold settings?
12. Consider another example where four aggressor nets can cause a rising glitch when the aggressor nets transition. Evaluate the worst possible combination of aggressor switching which results in the largest glitch?